SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

High Speed Digital: How to Optimize a Probe Card for PAM4 Signaling to a non-50 Ω device

Daniel Bock, Ph.D.

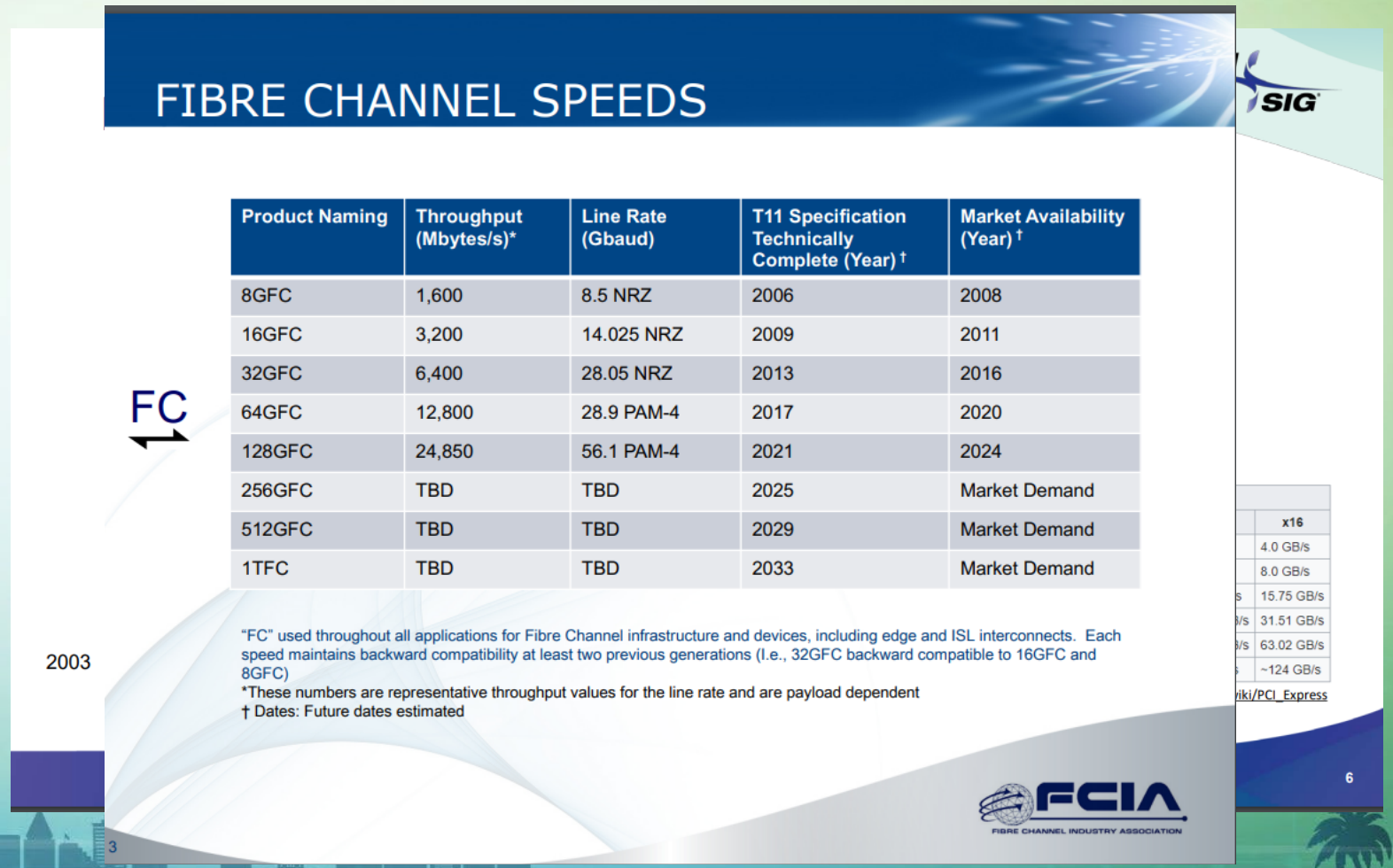
FormFactor

Agenda

- **Introduction**
- **What is High Speed Digital**
- **Process to optimize for non-50 Ω environments**
  - Selection of probe card technology
  - Optimization of layout
  - Transmission line Z
  - Component values
- **Comparison of model to measurements**
- **Recommendations**

Where are the Highest Speed Digital Signals?

- **We have been talking about PCIe 6.0**
  - Single Channel speed of 7,800 MB/s
  - FFI probes this at wafer sort with our vertical technology
- **Fiber is up to 24,850 MB/s today**



FIBRE CHANNEL SPEEDS

Product Naming	Throughput (Mbytes/s)*	Line Rate (Gbaud)	T11 Specification Technically Complete (Year) †	Market Availability (Year) †
8GFC	1,600	8.5 NRZ	2006	2008
16GFC	3,200	14.025 NRZ	2009	2011
32GFC	6,400	28.05 NRZ	2013	2016
64GFC	12,800	28.9 PAM-4	2017	2020
128GFC	24,850	56.1 PAM-4	2021	2024
256GFC	TBD	TBD	2025	Market Demand
512GFC	TBD	TBD	2029	Market Demand
1TFC	TBD	TBD	2033	Market Demand

FC

2003

"FC" used throughout all applications for Fibre Channel infrastructure and devices, including edge and ISL interconnects. Each speed maintains backward compatibility at least two previous generations (I.e., 32GFC backward compatible to 16GFC and 8GFC)

*These numbers are representative throughput values for the line rate and are payload dependent

† Dates: Future dates estimated

FCIA FIBRE CHANNEL INDUSTRY ASSOCIATION

3

SIG

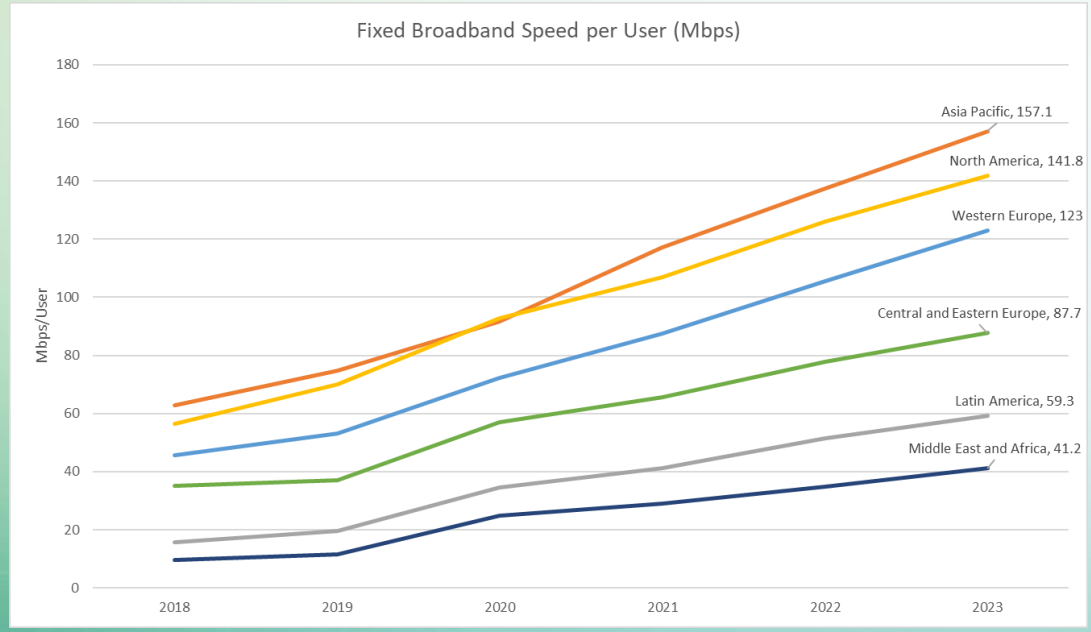
	x16
	4.0 GB/s
	8.0 GB/s
s	15.75 GB/s
B/s	31.51 GB/s
B/s	63.02 GB/s
	~124 GB/s

iki/PCI_Express

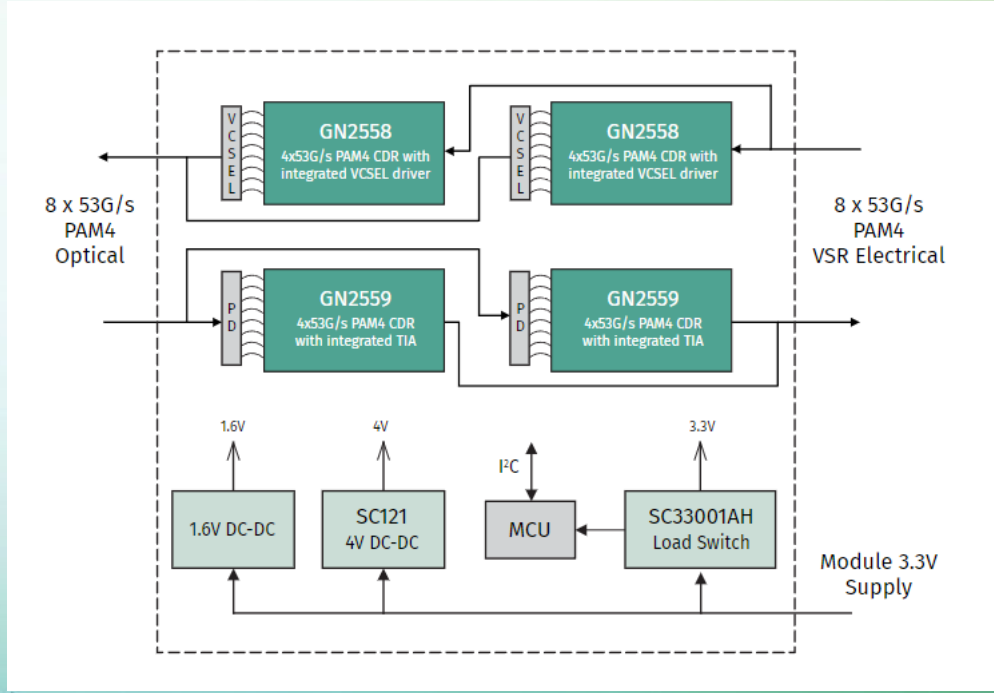
6

Fiber Communication Expansion

- **Data communication over fiber is requiring ever increasing speed in optical transceivers**
  - From 2015 to 2021, there is an increase of almost 2.5 times in the bandwidth per user over that time
- **To expand the telecommunications bandwidth, 100-400G TIAs, Laser Drivers, CDRs, and Active Optical Cables are available to help expand the bandwidth**



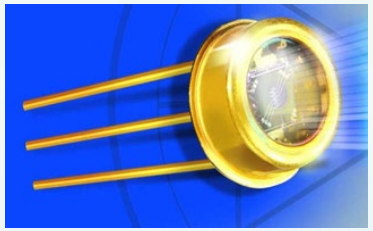
https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html



SEMTECH example 400G module that is part of an Active Optical Cable:
https://www.semtech.com/applications/networking-communication/datacenters

One Problem with Fiber Communication…

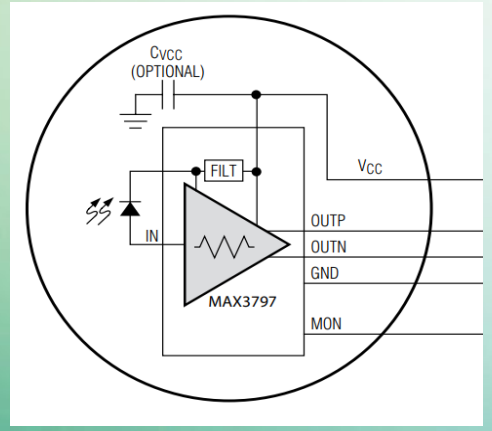
- **Unlike most digital systems, the key components for fiber optic communication are NOT 50 Ω**
  - Photodiodes – They are current sources, looking like a high impedance device



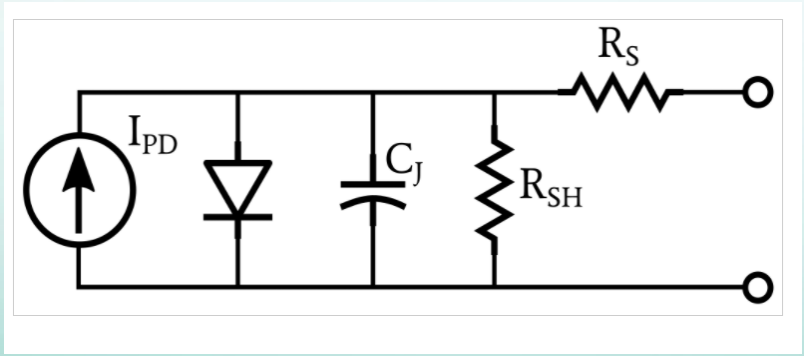
  - Laser Diodes – They are a current sink, acting as a low impedance load

Effects of non-50 Ω devices

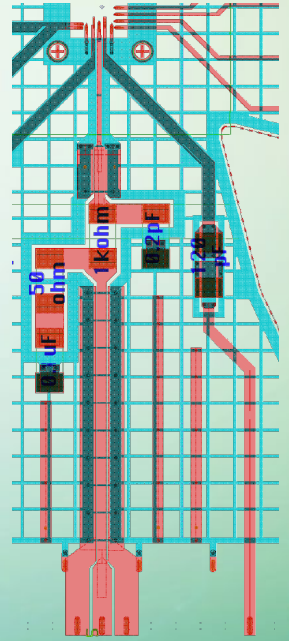
- **For High-Speed Digital devices, like TIAs, the input to the device is a photodiode**
  - The matching circuit on the probe card is designed to emulate the characteristics of the photodiode
    - This provides the most accurate wafer test



Application circuit, with photodiode



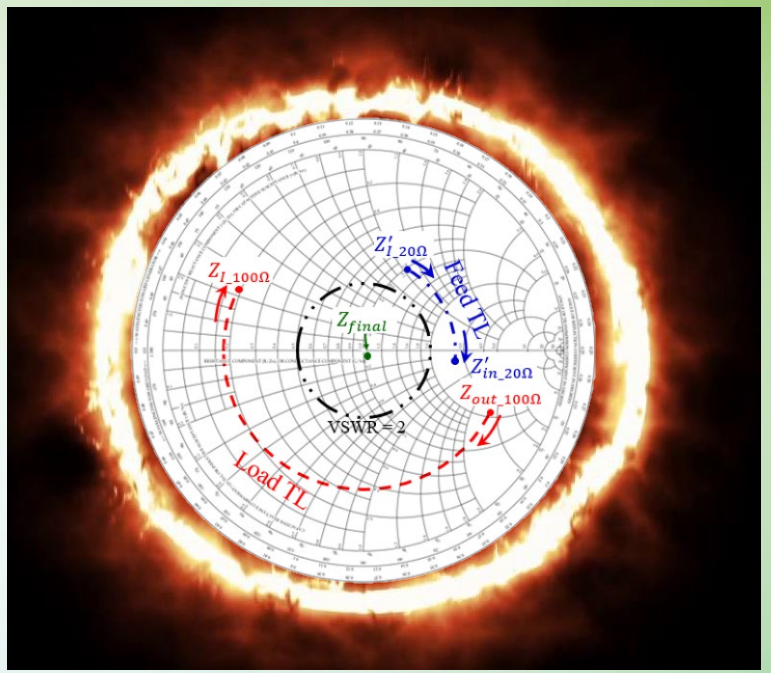
Photodiode equivalent circuit

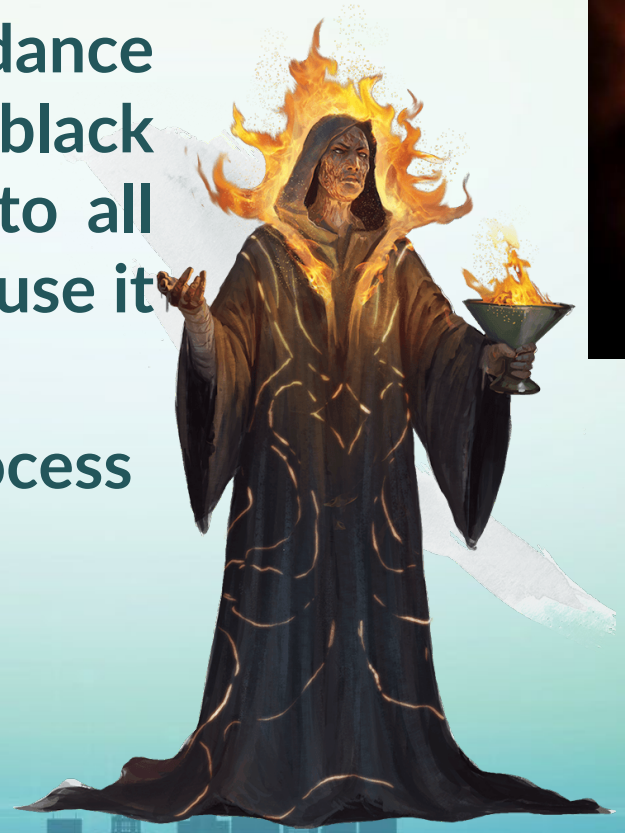


Photodiode emulating circuit

How do you design for these devices?

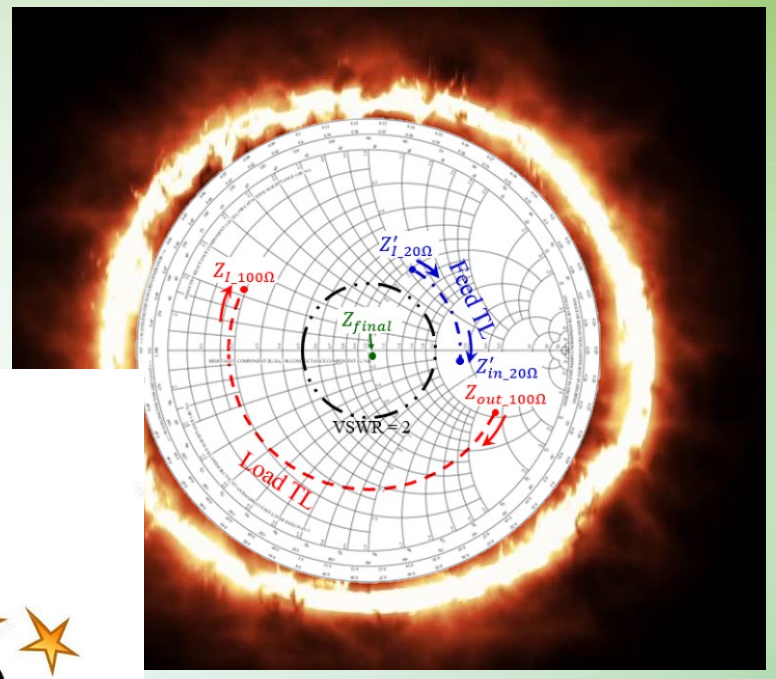
- In order to design for these devices, impedance matching methods in the digital signal path are required
- Many have described impedance matching (and RF in general) as ‘black magic’, something impenetrable to all but those most skilled in RF, because it feels non-intuitive
- FormFactor can help with this process





How to Demystify Impedance Matching?

- **Trying to take the magic out of the process, I will go over:**
  - What input information do you need to make a matching circuit?
  - What are the process steps optimize a matching network?
  - How to validate the matching without the customer device?



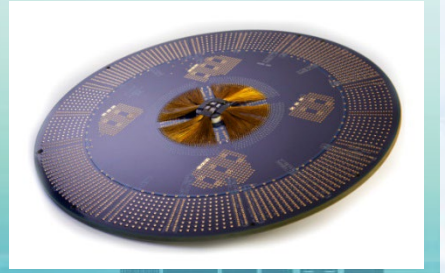
What do we need to simulate the Device?

- **Beyond the normal DUT layout inputs, some additional information can help:**
  1. Selection of the probe card technology
  2. Circuit schematic information for matching circuit
     1. Typically evaluation board circuit
  3. Model of the Driver circuit
  4. Performance model of the DUT
     - S-parameter model is best; or,
     - Z of the device is minimum

Which Probe Card Technology?

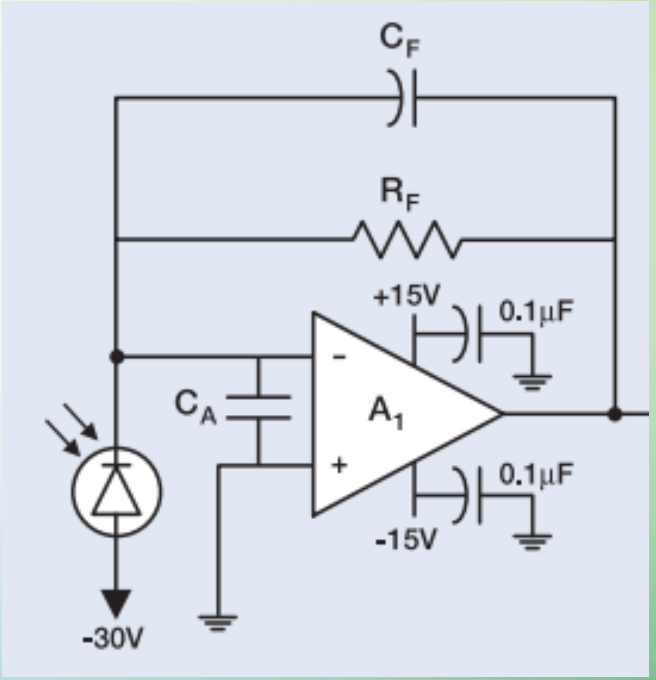
- **The key parameters for high speed digital devices include:**
  - Speeds > 60 GHz
    - Channel count of a single DUT is typically between 6-32 RF lines, and do not require multi-DUT due to tester limitations
  - Pitch of ~ 120 µm, periphery
  - Impedance matching circuits close to the DUT, as well as non-50 Ω transmission lines before the matching circuit
    - Impedance matching can be supported by all Pyramid Probe core sizes for single site to multi-site applications in order to emulate package test

	Cantilevers	Vertical MEMS	Spring Pins	Pyramid Probe
RF Signal Performance	< 3 GHz	< 40 GHz	< 55 GHz	> 80 GHz
Pitch (Periphery)	40 µm	90 µm	150 µm	80 µm
Max Size	90 x 20 mm	100 x 100 mm	90 x 20 mm	10 x 80 mm
Distance from DUT for Matching	> 4 mm	> 3 mm	> 3.5 mm	> 1 mm
Design non-50 Ω Transmission line	No	No	No	Yes



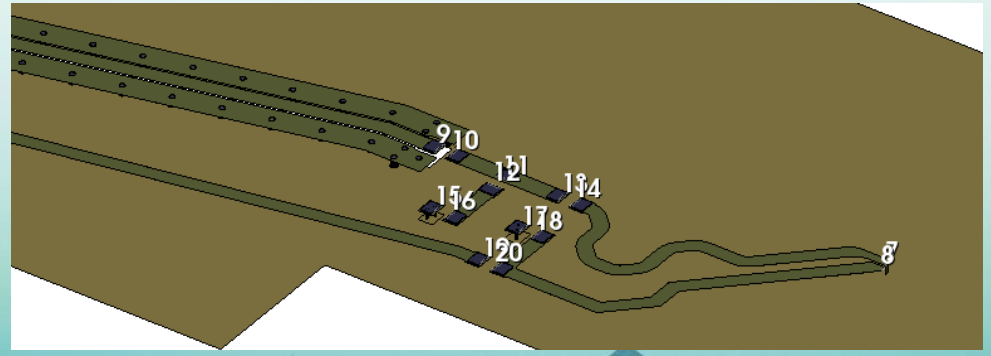
Input Circuit Schematic

- **Providing a known circuit is a good starting point**
  - Designers provide details in application notes that give desired values for the components that give optimized performance in final package



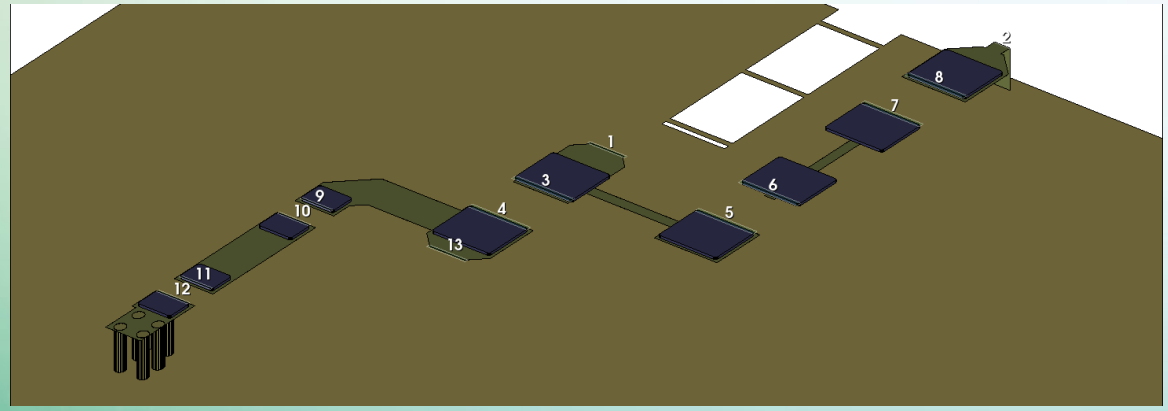
Initial Design

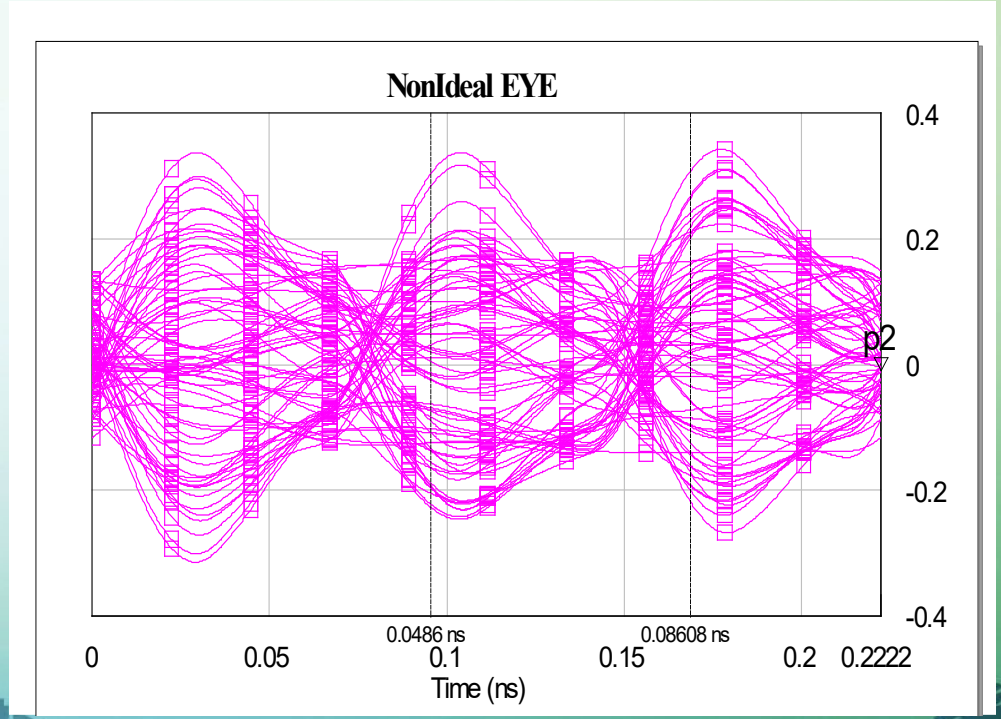
- **In order to optimize, a probe card designer would layout the circuit using the inputs from the customer, as well as design rules**
  - These will typically not provide the best performance, but act as a starting point



Matching Circuit Footprint

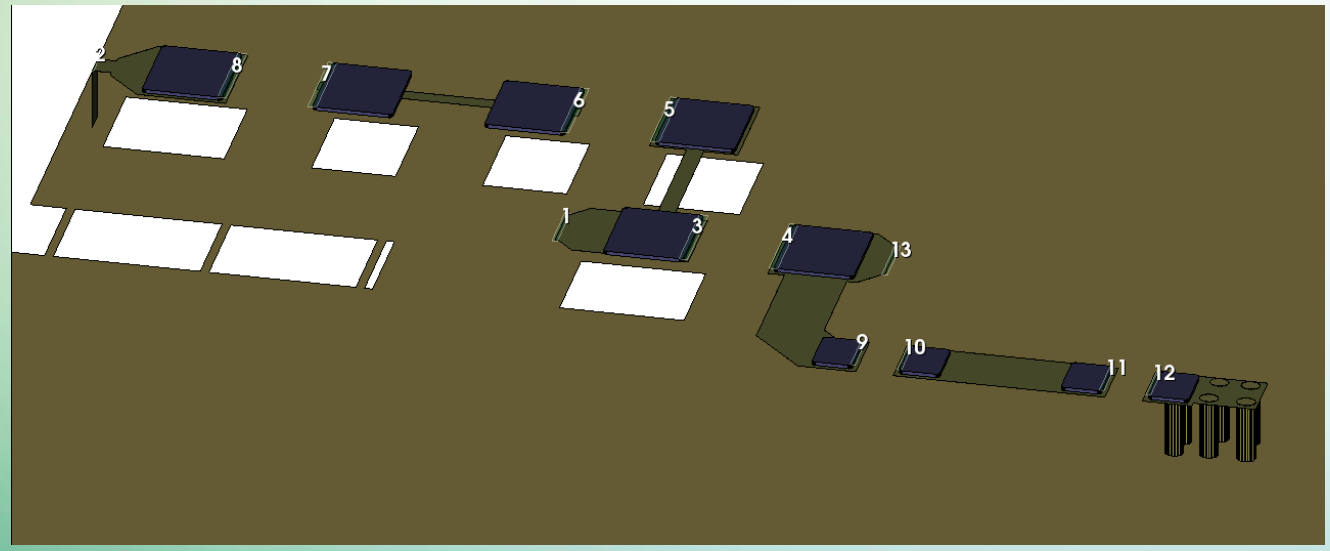
- **The first analysis looked at the matching circuit, and the pad structures**
  - The eye was closed completely prior to optimization

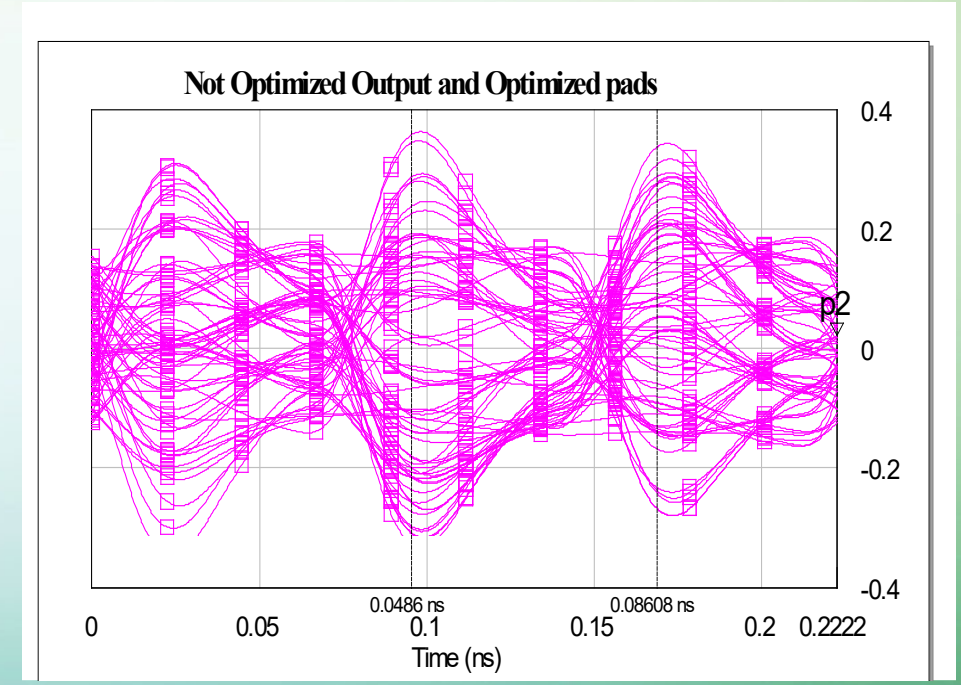




Optimizing the Pads

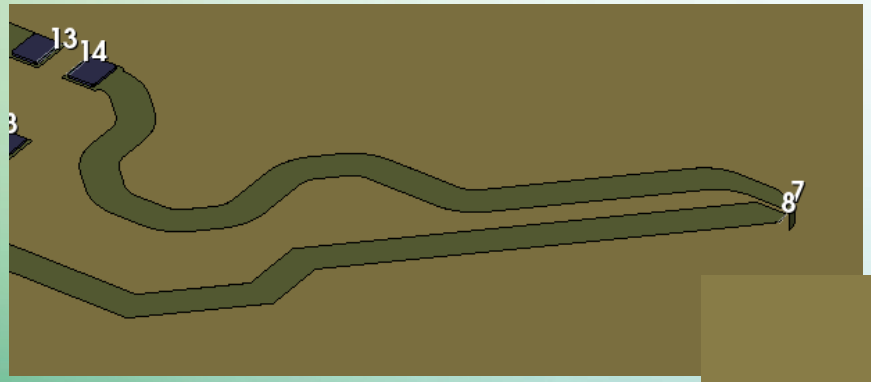
- Once we optimized the pads, it started to look better, but still not ideal

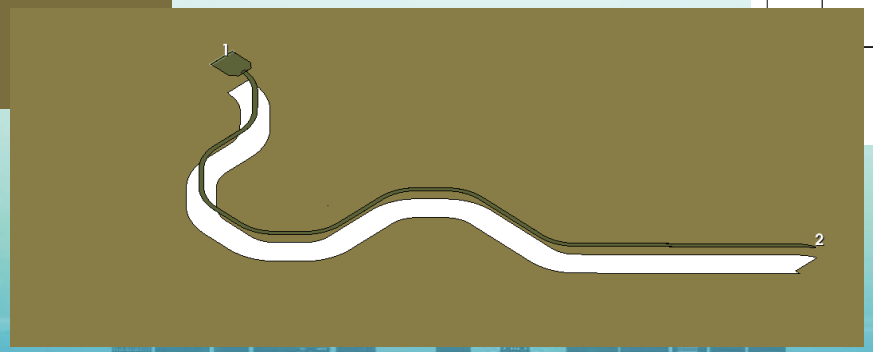


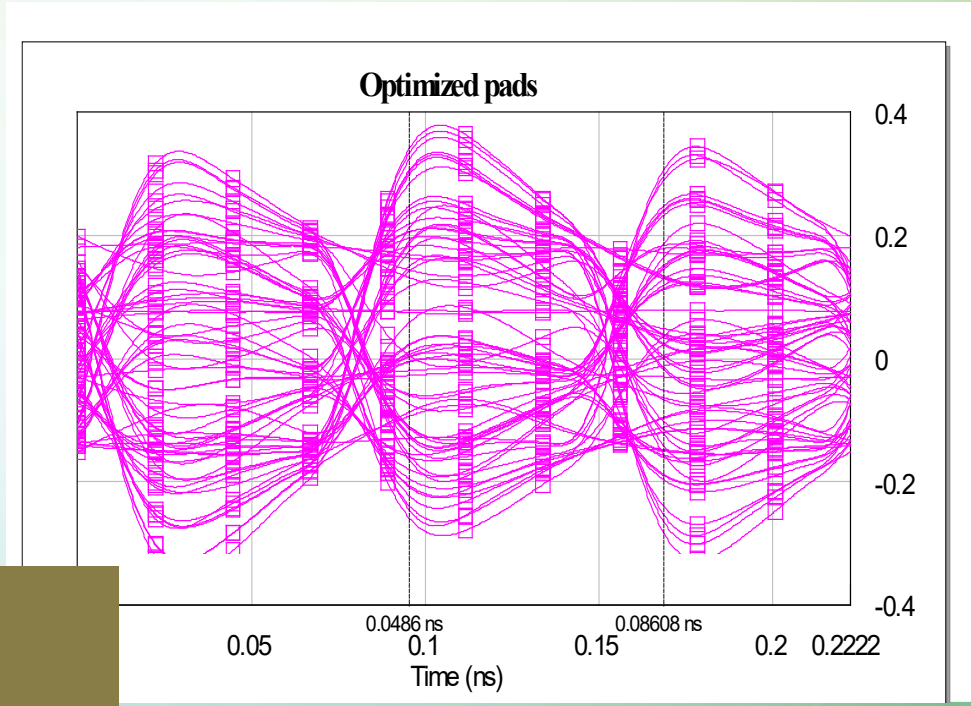


Trace from Network to DUT

- **The input trace from the DUT into the matching network needed optimization based on the eye performance**
  - First design was too low impedance

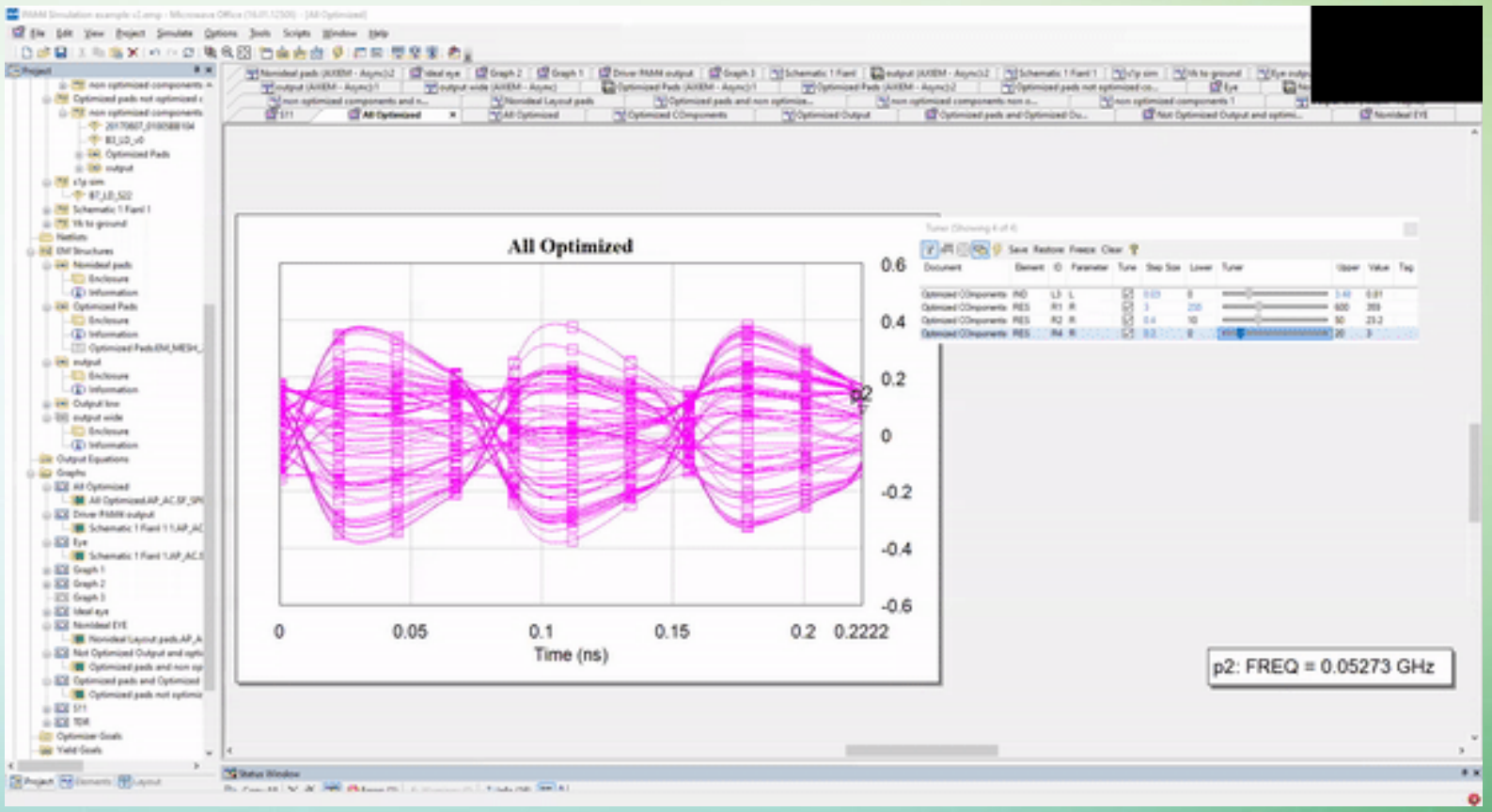






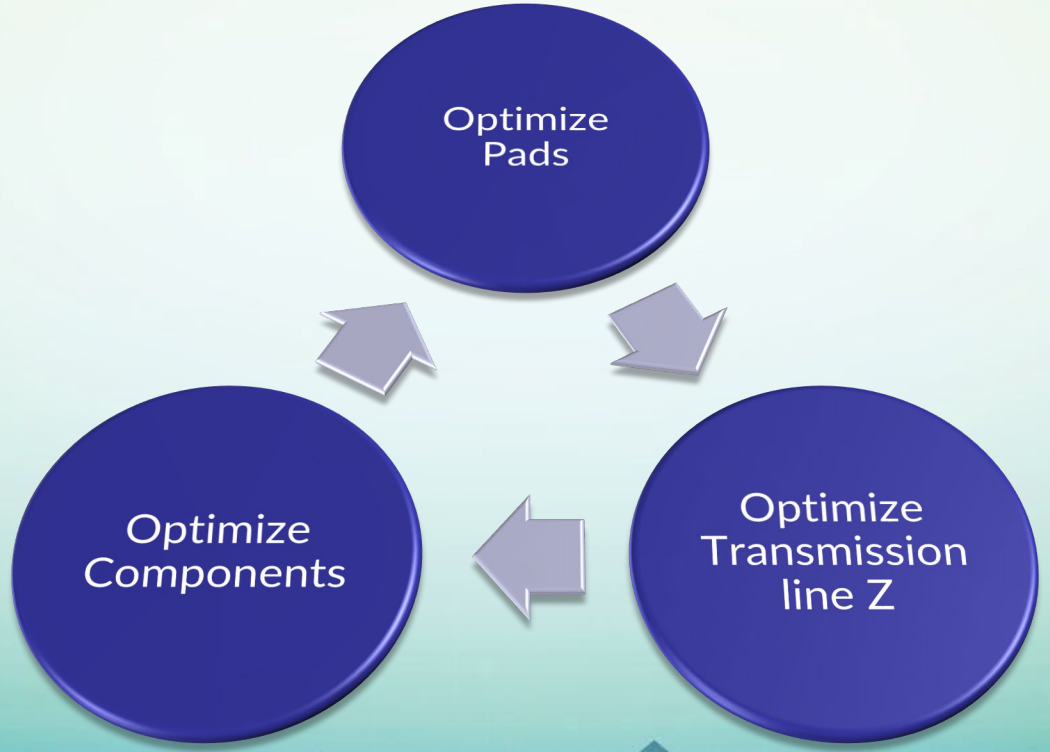
Optimization of the Components

- **Typically, certain components are more important to maintaining a good eye than others**
  - Vary them all until you know which components are most important, and then optimize those



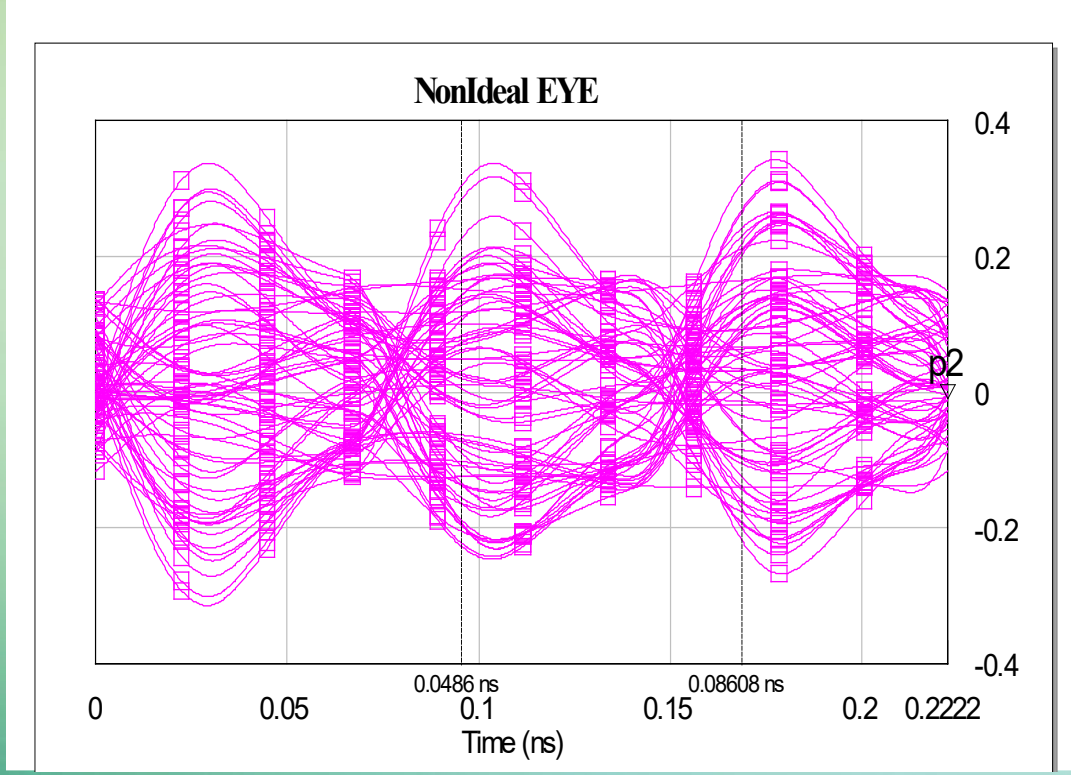
Repeat Process as Needed

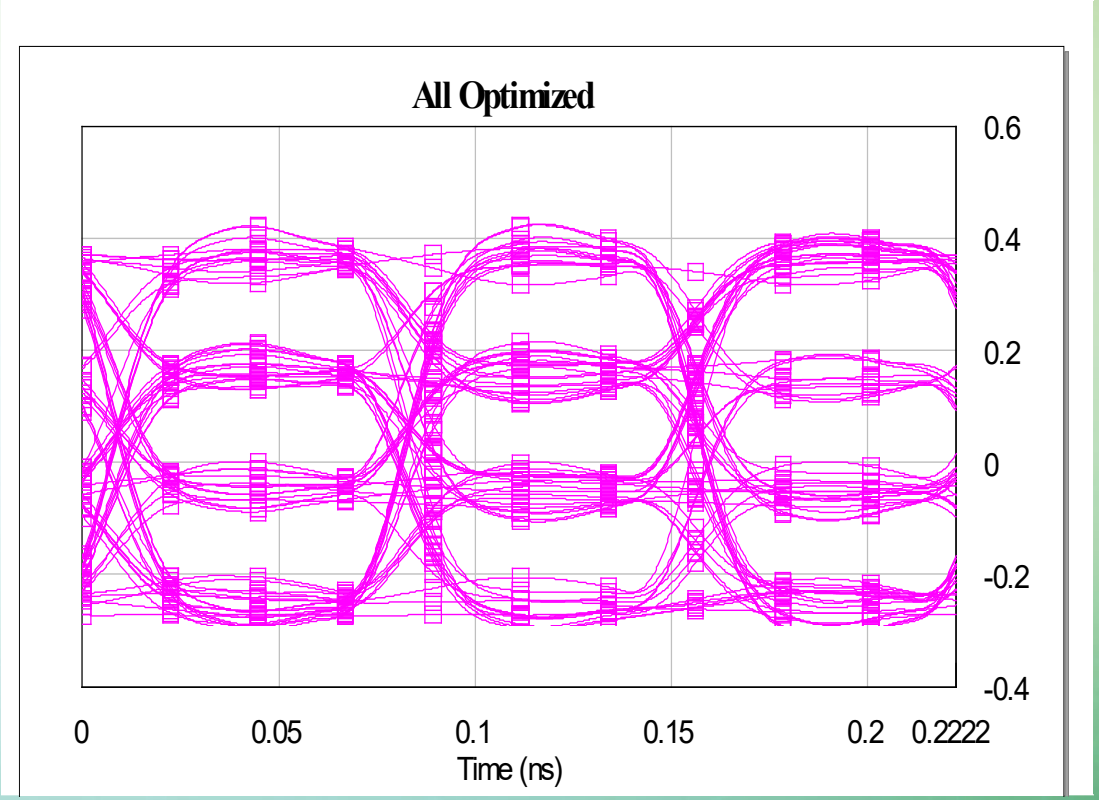
- Typically, this requires multiple cycles through each step until the best parameters are found for the largest eye



Final Optimized Eye

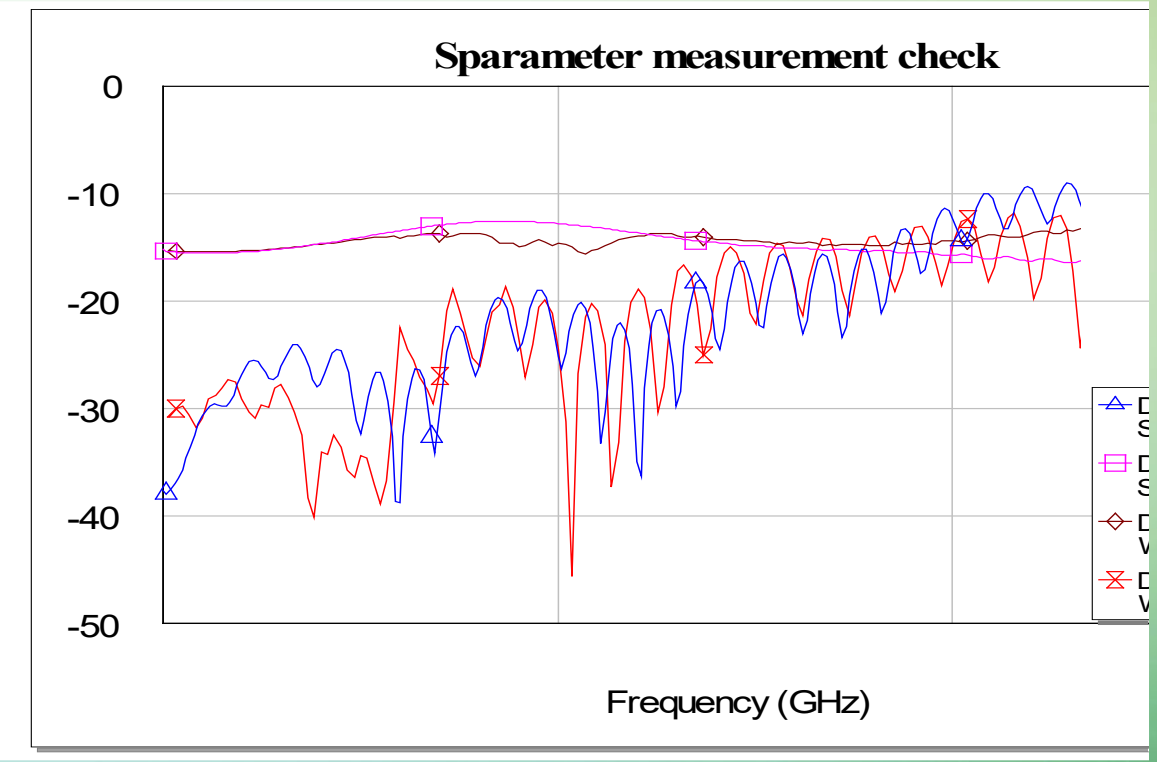
- Results after optimized design is completed





Final Check – RF Measurements

- **The last step was to compare the S-parameters of the probe head from simulation to measurement to confirm design**
  - It showed great correlation between the two

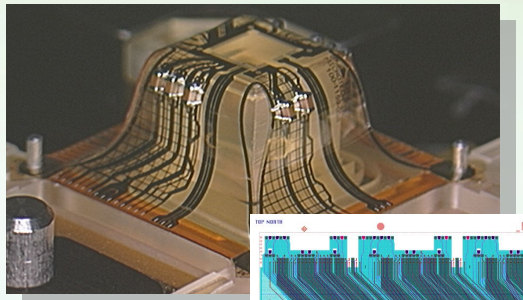


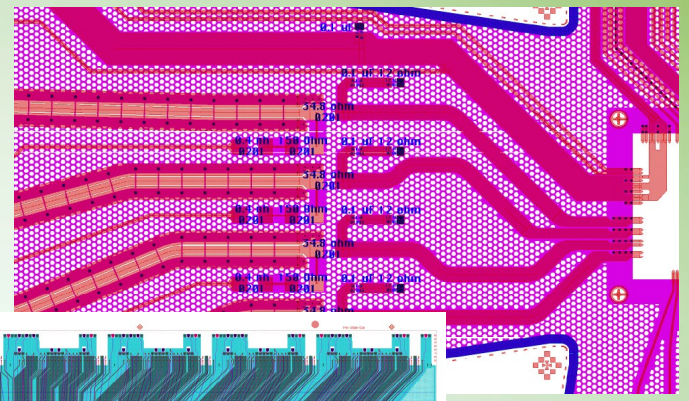
Outlined the Procedure for Optimizing

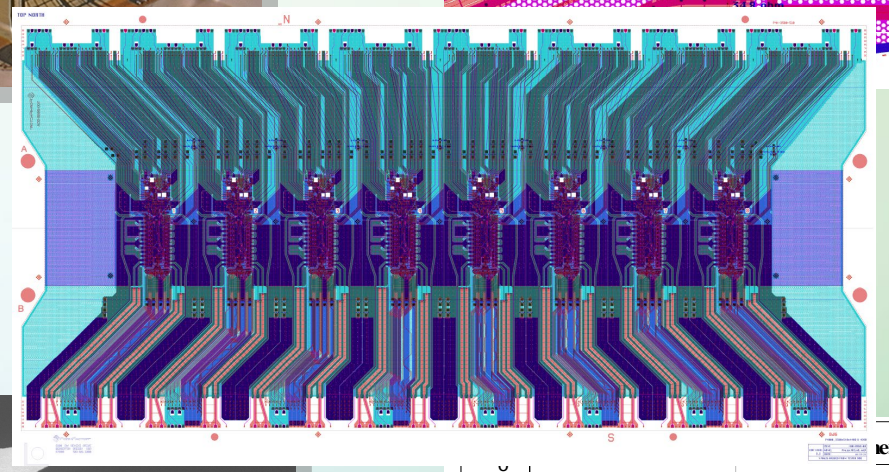
- **The Procedure for Optimizing includes:**
  - Selection of the proper probing technology for the DUT type
  - Collect design information to model the DUT
  - Optimize the following until the desired performance is reached:
    - Matching circuit footprint
    - Input trace from the DUT
    - Component values for the matching circuit

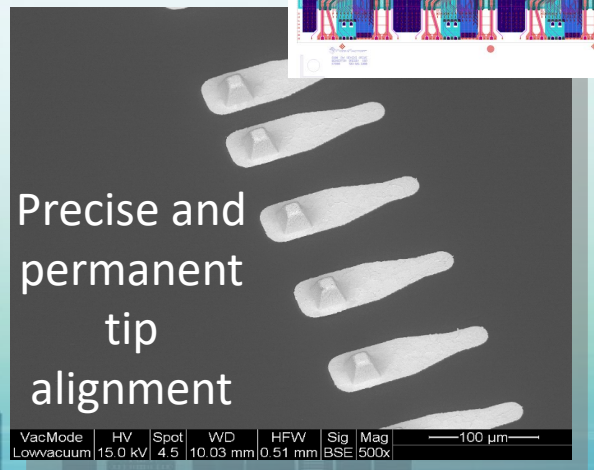
Pyramid Probe– Best Performance

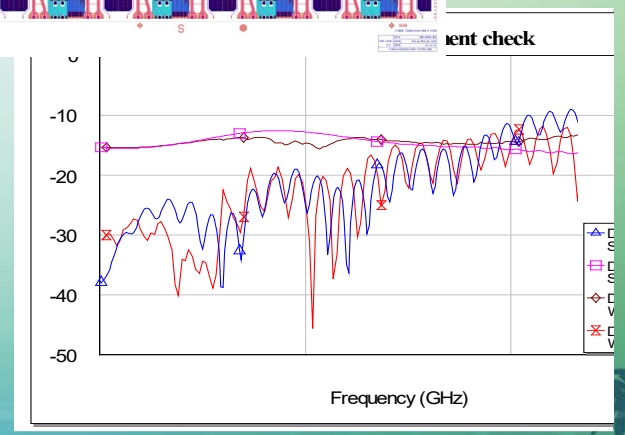
- **Integrated Probe Tip and Space transformer**
  - Lower loss and better RF transition for best signal integrity
- **Low Inductance Contactor**
  - Up to 81 GHz bandwidth, highest of any wafer probing technology on the market
- **Best RF Circuit Performance**
  - RF circuit design possible within 1 mm of the probe tip
- **Tunable transmission line Z**
  - 5 Ω – 100 Ω
- **RF Calibration Capability with ISS**











Questions