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Key Design Parameters to Maximize Probe Current Carrying Capability

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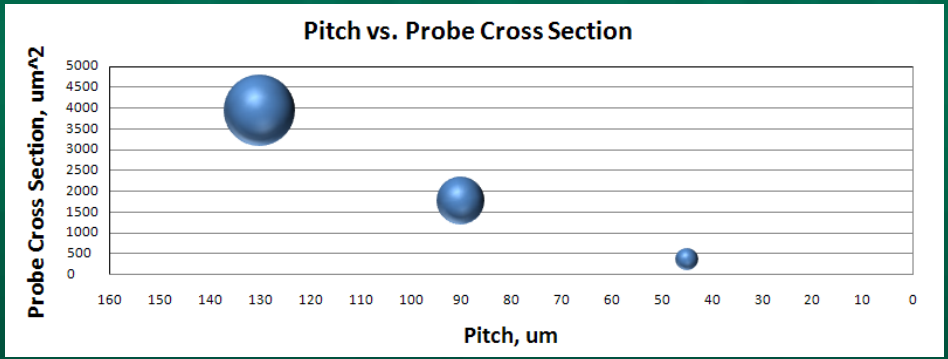
Overview

- Key System-on-a-Chip (SoC) Semiconductor Trends Influencing Probe Current Carrying Capability (CCC)
- Definition of CCC
- Variables Affecting CCC
- Trade-offs Between CCC, Probe Deflection Range, and Inductance
- Example of Optimized Solution
- Summary

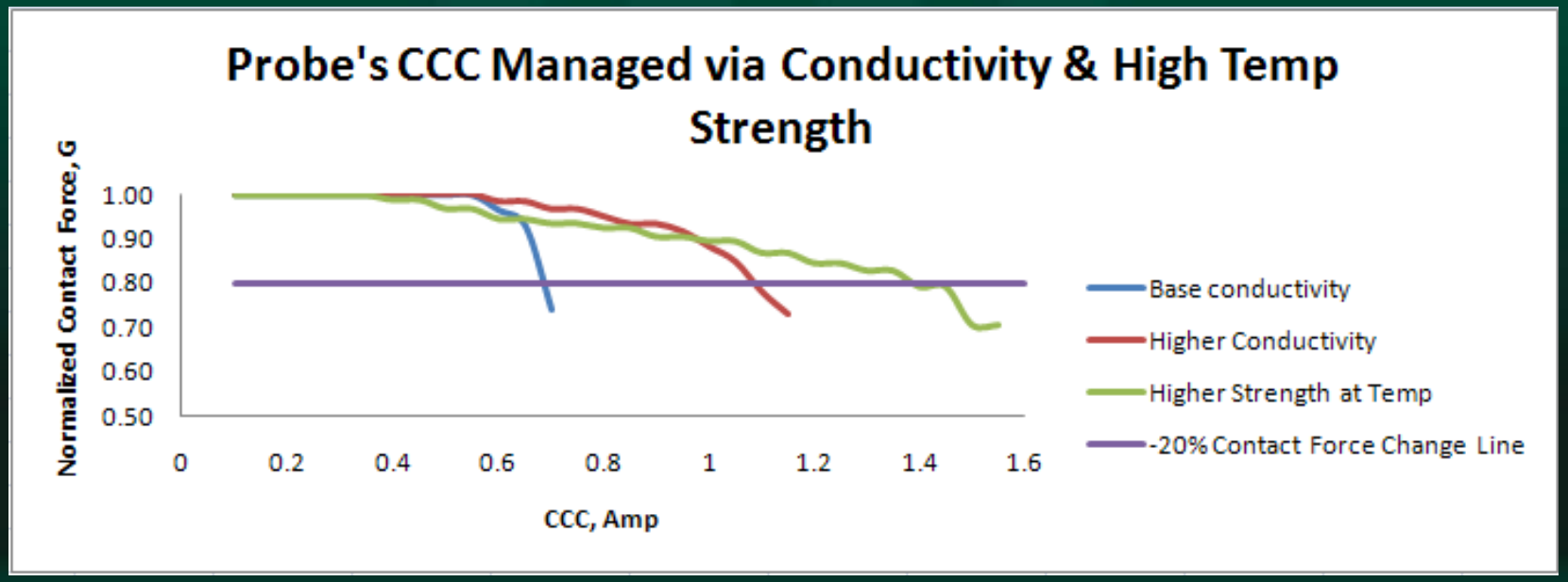
Key Semiconductor Trends Influencing CCC



- **Geometries Are Getting Smaller**
  - Logic/SoC full-grid-array pitches continue to shrink from today's 130µm to sub-100µm by 2016 (ITRS roadmap)
  - Thru-silicon-via (TSV) technology will require sub-50um pitch in full-grid arrays before 2013
- **Current Densities Are Increasing**
  - Transient currents can be significantly higher than 0.5A/probe
  - CCC of ~1.0Amp per probe required for production robustness
- **The Challenge: Carrying More Current Through An Ever-Shrinking Cross-Section**

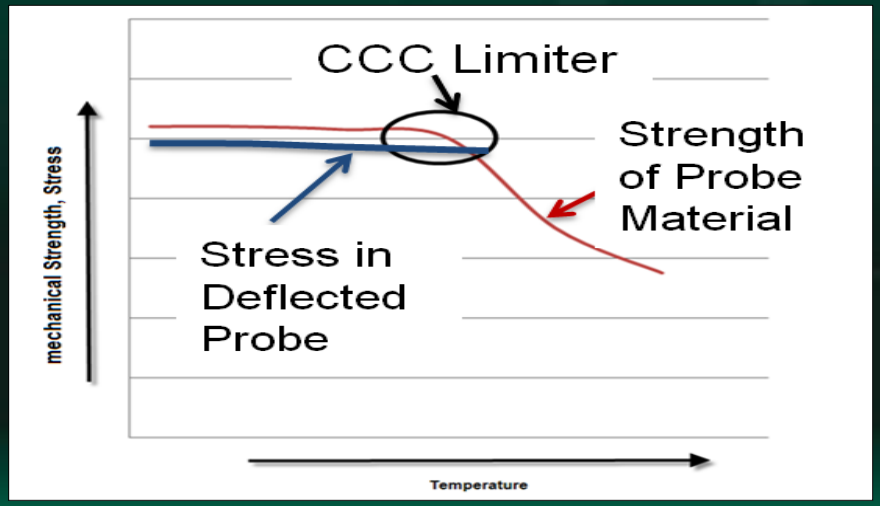
Definition of CCC

- **CCC = Current which results in a 20% contact force reduction**
  - Below plot typical of SEMI-defined methodology
- **CCC modulated by several variables**
  - Here, improvement achieved through probe material conductivity (electrical and thermal) and high temperature strength increase



Variable 1: Probe Material Properties

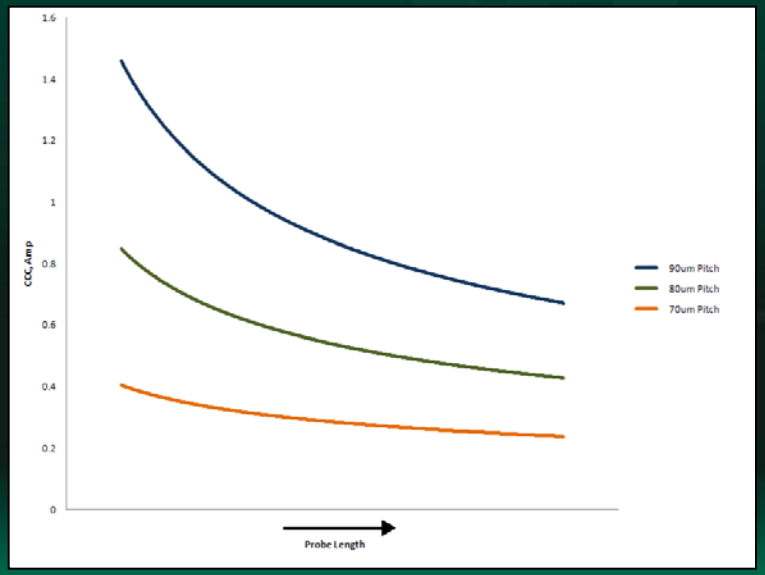
1. **Bulk resistivity**
   - Lower resistivity lowers temperature rise from Joule (I^2R) heating
2. **Yield and fatigue strength (at elevated temperature)**
   - High mechanical strength at elevated temperatures better supports probe deflection stress at operating conditions
3. **Probe tip metallurgy**
   - Lower Cres = Improved CCC (as we will see in Variable #5)



Mechanical strength of typical spring metals diminishes rapidly past critical temperature marked here as "CCC limiter."

Variable 2: Probe Geometry

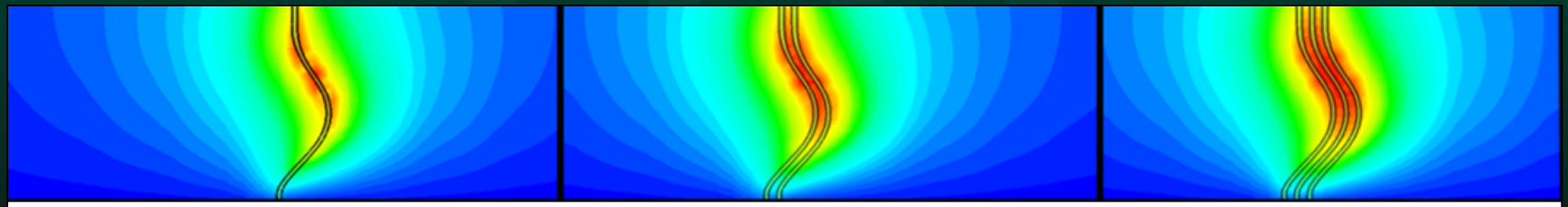
- **Probe Cross Section (pitch) – A BIG EFFECT!**
  - Slender probes (ie, probes at smaller pitch) have reduced CCC because of:
    - Higher stress
    - Higher electrical resistance
    - Lower convective heat transfer
- **Probe Length**
  - Shorter probes offer higher CCC because of shorter distance to heat sinks



Example relationship between probe CCC and probe length for 70, 80, and 90µm pitch in full grid array layouts

Variable 3: Probe Layout

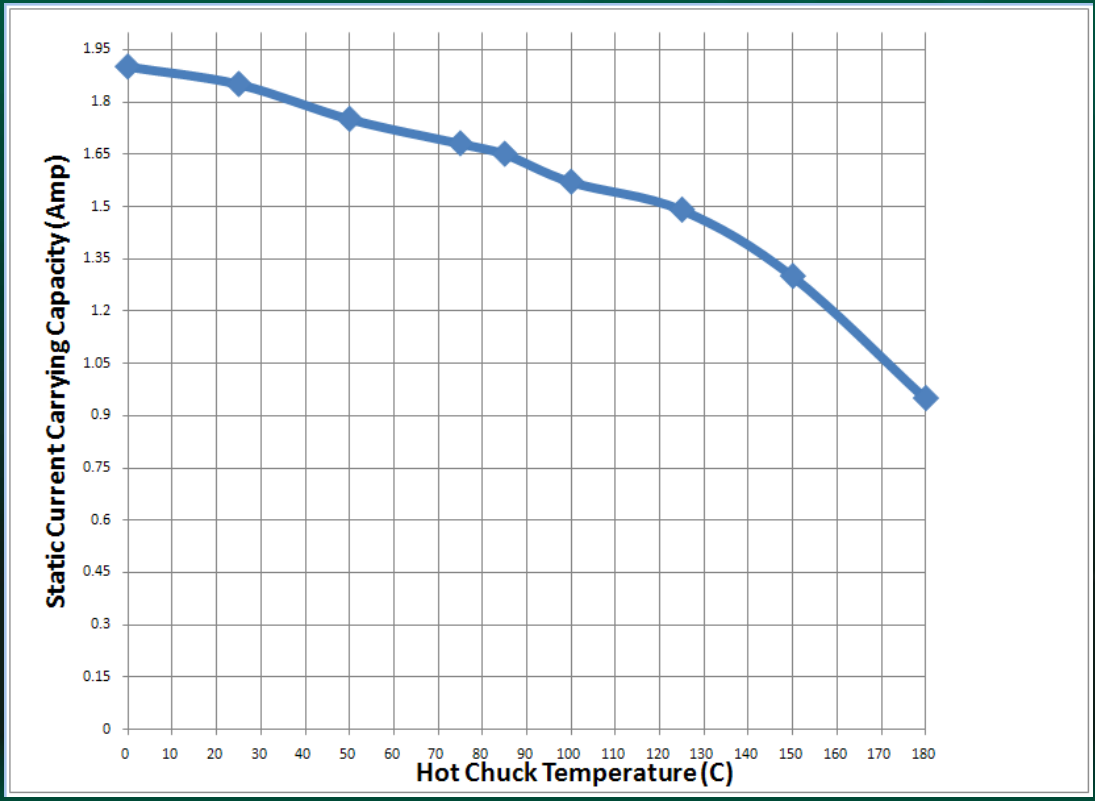
- **Example:**
  - Single isolated probe measures 1.05Amp CCC at room temperature
  - Add a neighbor 130µm away, CCC drops to 0.95Amp
  - Add another neighbor 130µm away, CCC drops to 0.91Amp
- **In a 3x3 matrix at 130µm pitch, center probe CCC is 0.89Amp**
  - 15% reduction in CCC from isolated single probe



Influence of neighboring probe proximity on CCC at 130µm pitch. Color indicates temperature distribution (red = hot).

Variable 4: Chuck/Wafer Temperature

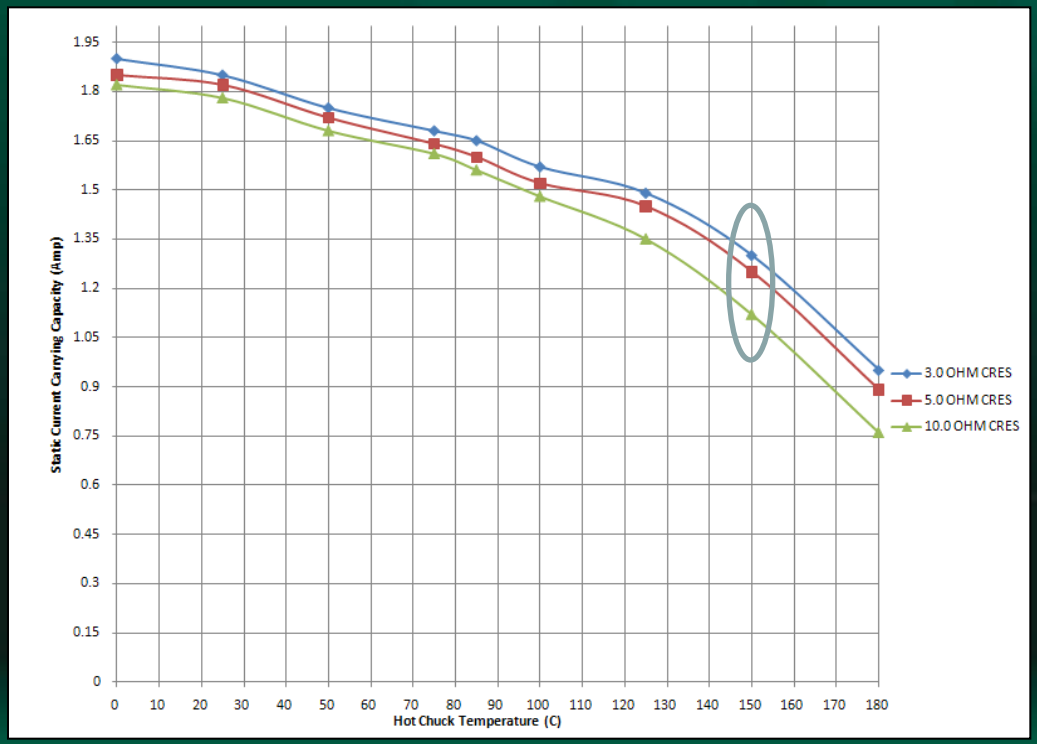
- **Example: 1.9Amp CCC @ 25C degrades to 0.9Amp CCC @ 180C**
  - Higher temperature inhibits heat transfer from probe
  - Reduced heat transfer = Decreased Probe CCC



- CCC as a function of wafer temperature
- Data for 75µm probe deflection

Variable 5: Probe Tip Contact Resistance

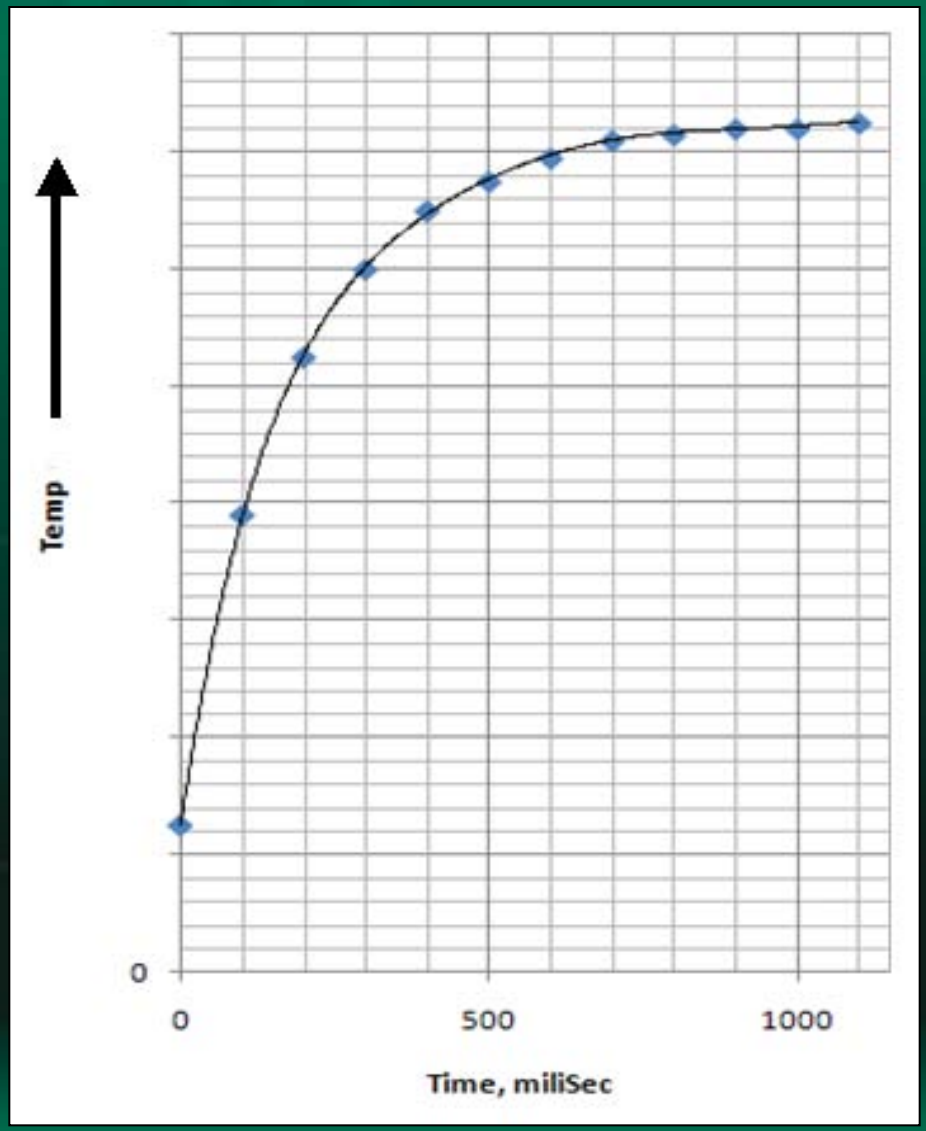
- **Example: 1.3Amp @ 3Ω Cres drops to 1.12Amp @ 10Ω Cres**
  - Tip-to-pad resistance increases local heat generation through I^2R losses and decreases local thermal conductivity through material property changes
  - Increased heat generation & reduced heat transfer = Decreased Probe CCC



- CCC as a function of wafer temperature and Contact Resistance
- Data for 75µm probe deflection

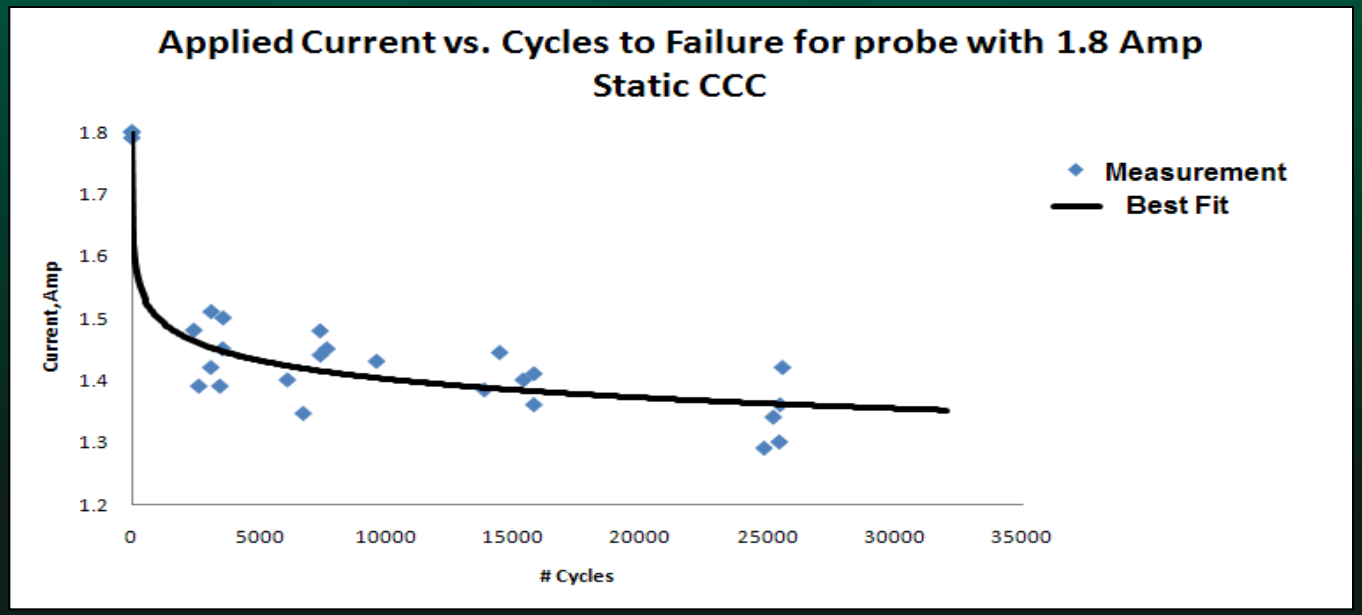
Variable 6: Electrical Duty Cycle

- Typical probes reach steady-state temperature in under 2sec
- For shorter current-ON intervals should consider equivalent DC current and from there the required CCC value



Variable 7: Dynamic Cycling

- **Example: 1.8Amp CCC reduced to 1.4Amp if 10k Cycles required**
  - Determines not only what current level a probe can carry one time, but also how many cycles a probe can sustain at various current levels below the static CCC



Example of dynamic CCC test result correlating current to number of achievable probing cycles for a probe with 1.8Amp static CCC

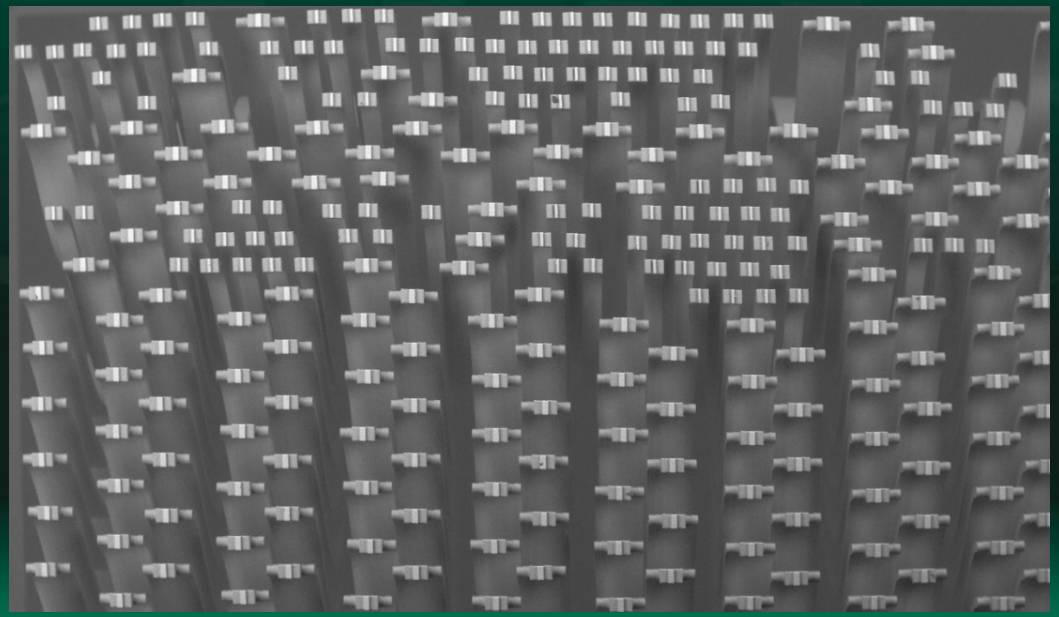
The Trade-Off: CCC, Deflection, and Inductance

	Short Probe	Long/Slender Probe
Advantages	• High CCC • Small Self-Inductance (high frequency)	• Large deflection range (able to absorb large bump co-planarity)
Disadvantages	• Small deflection range (unable to absorb large bump co-planarity)	• Low CCC • Large Self-Inductance

- **As with most engineering problems, significant tradeoffs exist in satisfying all requirements**
  - High CCC = Small self-inductance, poor compliance

Example of Optimized Solution

- **Dual-probe design with composite (multi-material) probe structure**
  - Independent optimization of power, ground, and I/O probes
  - Satisfy multiple requirements, while “deconstraining” from a single-probe design



Summary

- **Production-worthy SoC probe cards must satisfy competing mechanical and electrical requirements**
  - Current Carrying Capacity (CCC) becoming increasingly challenging as pitches shrink
- **Requirements can be mutually exclusive with a single-probe, single-material design**
  - 1Amp/probe in sub-100µm array configuration benefit from a Multi-Probe (each with multiple composite layers) design
  - Allows for independent optimization - maintain highest CCC performance, while not compromising I/O performance
- **Effective probe tip cleaning protocols become even more critical in maintaining the best CCC during production**