IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

Expanding Test Coverage at Sort to Reduce Overall Product Costs

FormFactor
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Agenda

- Product Studies
- Card Attributes/Life Study
- Cost of Ownership
- Next Steps
- Summary

Product Studies

- **Probe Head specification vs. Cantilever**
- **High speed product evaluation**
  - 1.6GHz
  - Al pads
- **Power management evaluation**
  - 1.5 Amps
  - Copper pads
- **1st Production Version**
  - Beat production schedule

MEMS vs. Cantilever Probe Specifications

MEMS Specification

- **Probe Inductance 1.1 to 1.3nh**
  - Typical Probe 2.4mm in length
- **Planarity +-10um**
  - Actual part +/-5 um
- **Probe life >1million**
- **Controlled Z probe launch**
- **Passive Components mount on Probe Head**
- **Current carrying capability 0.5A**
  - Actual 1.5A on 2 probes

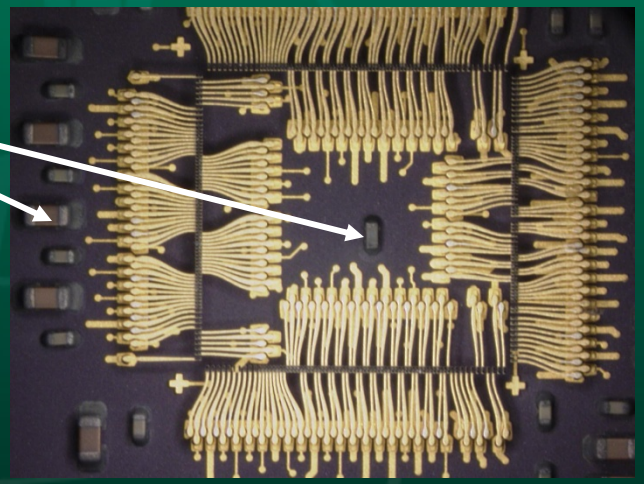
Cantilever Specification

- **Probe Inductance 27nh / inch**
  - Typical Probe 1 inch in length
- **Planarity +-15um**
- **Probe life ~1million**
- **Controlled Z to PCB Launch**
- **Passive Components on PCB**
- **Current carrying capability 200mA with 25um tip**

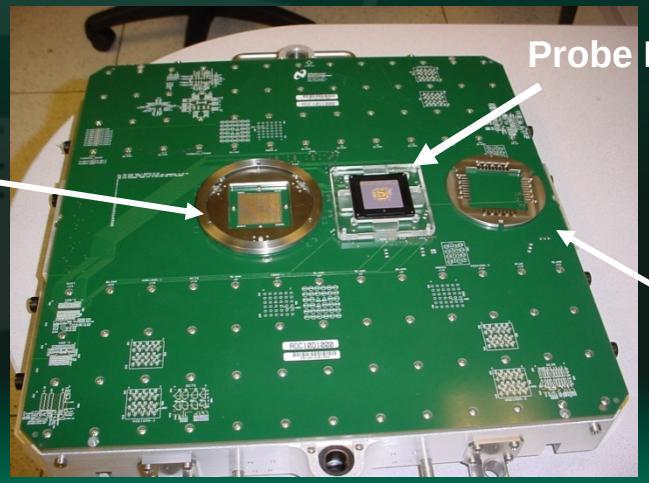
High Speed Probe Head Hardware

- **Critical Passives on Probe Head**
  - 48 components on ADC PH
- **78 Matched transmission line length on Probe Head**
  - Includes probe length
  - Used PCB to compensate groups
- **EZ to assemble and exchange probe head**
  - Mechanical Assembly
  - Probe Head
  - PH Cover
- **760 Pin I/O**

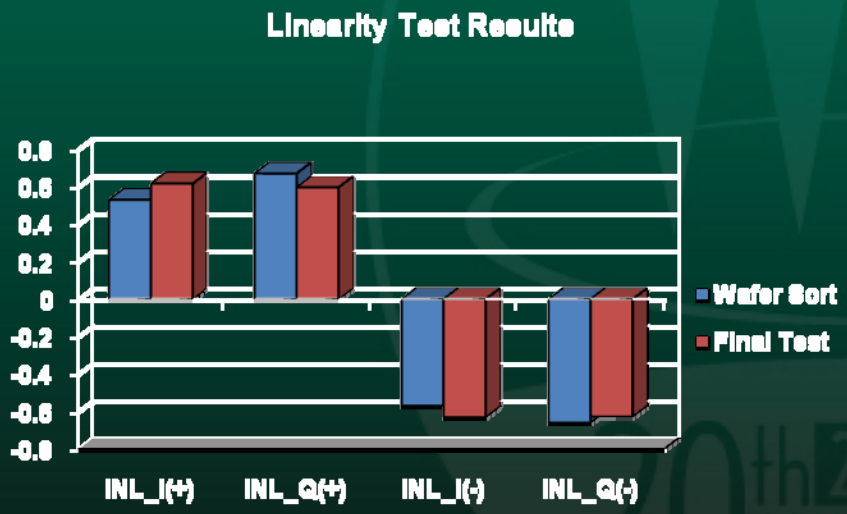
Probe Array

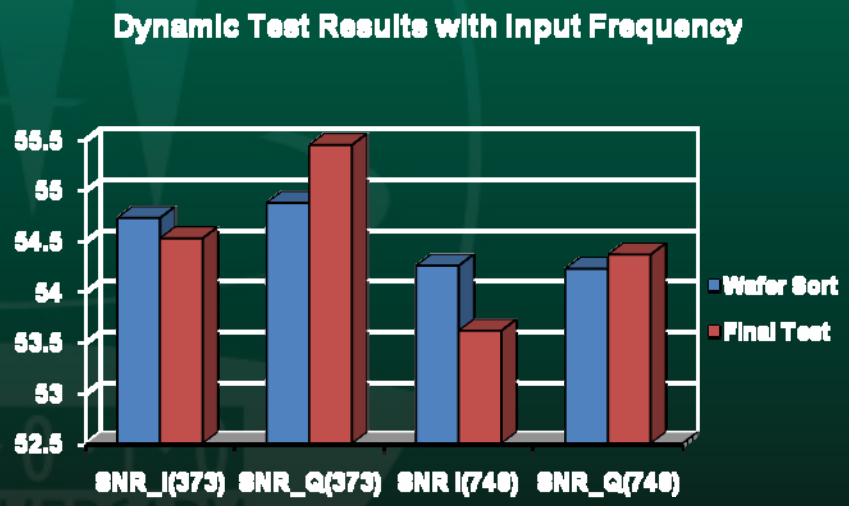


ADC / FormFactor DIB



Good Correlation Between Sort and Final Test

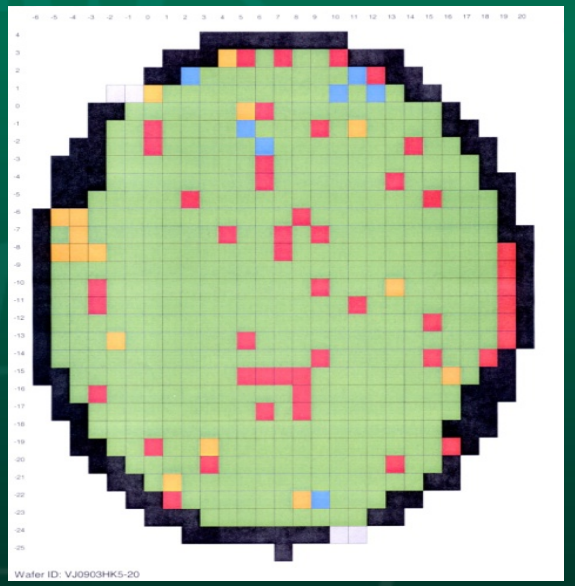


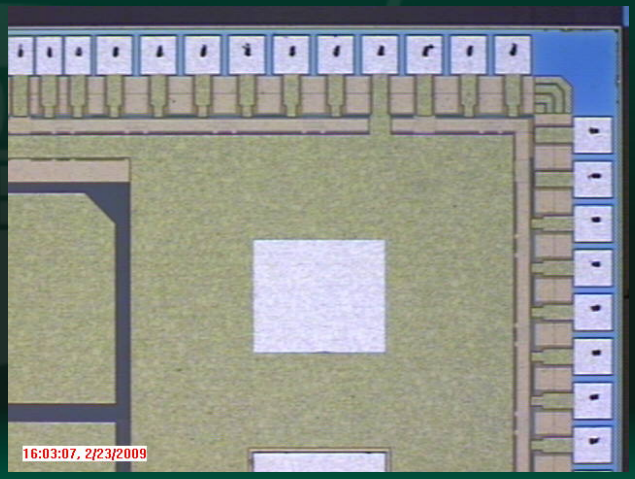


Not able to run these tests with Cantilever card

High Frequency Product Probe Card Test Results

- **Test Vehicle: High frequency AL pads**
  - Sampling rate 1.6 Gsps .
  - AC test input frequency
    - 250 and 750M.
- **Compared to currently released wafer sort solution**
  - Tests only continuity, voltage level and power supply current; no AC tests.
  - ~Equivalent yield.
- **Yield on MEMS probe card**
  - Equivalent yield Compared to Cantilever Test List
  - SNR and Linearity yield at Sort at 6%
  - Compared SNR and Linearity test at to FT results
    - ~6% yield loss due to AC test failures (SNR and Linearity)

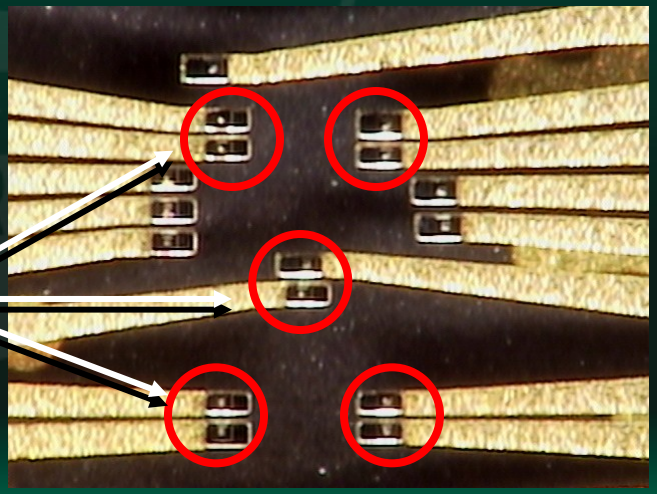




Power Management Device

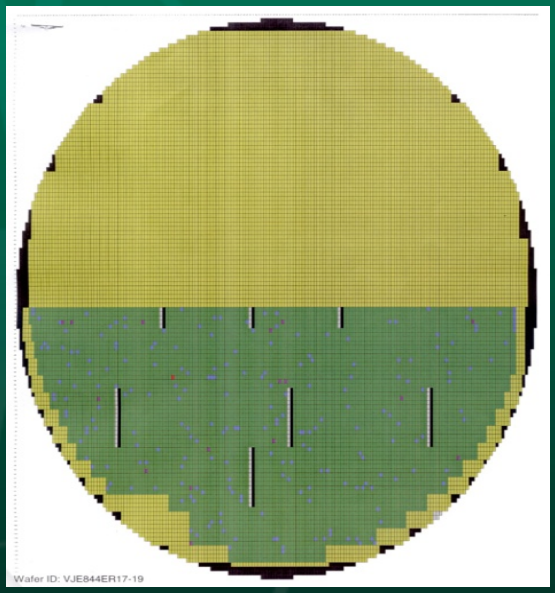
- **Compact Design**
- **Kelvin on 5 pins**
- **Components on probe head**
- **136 I/O connections**
- **Good contact on Copper Pads**
- **EZ setup / EZ replacement**
- **Can have multiple force pins**
  - 2 for and one sense pin on 180 x 68 um pad
- **Probe Head Configurable**
  - Multi Site

Probe Assembly as Tested



Test Results on Power Management Device

- **Single Wafer Sorted 8 times**
- **No probe pad damage on Copper**
- **Continuity stable**
- **RDSON Stable**
- **I_limit Stable**
  - Tests up to 1.5amps with two force pins



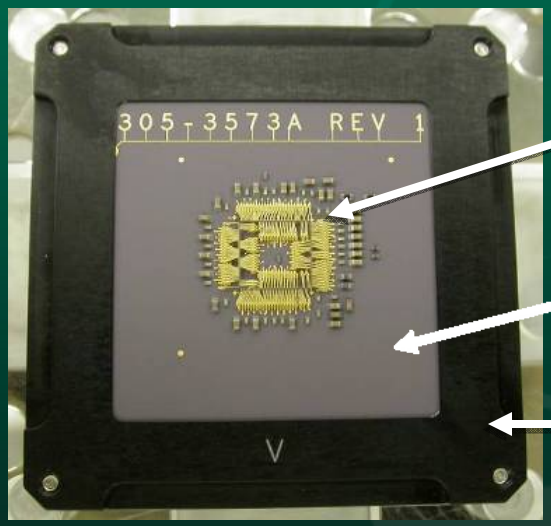
DATE	1/8/2009	
LOT#	VJE844ER10 to WJE844ER17	
Wafer	19	
Sort	Bottom half wafer, 8 times	
Temperature	Room	
PCB	Modified kelvin	
Product File	Mofidied to not touching edge dies	
		Bin 1 (%)
	VJE844ER10	96.92
	VJE844ER11	96.75
	VJE844ER12	96.85
	VJE844ER13	96.88
	VJE844ER14	96.85
	VJE844ER15	96.99
	VJE844ER16	96.94
	VJE844ER17	96.81
Note	There is no strip issue on all 8 sorts.	

Summary Initial Product Trials

- **Sort Improvements using MEMS Probes**
  - Better signal fidelity at die
    - Bypass, bias resistors, inductors, short probes, etc.
  - We can effectively test everything at wafer sort on both ADC and PM devices
  - Improved probe card life
  - Reduce scrap after value added steps
- **Tradeoffs**
  - Longer lead time for MEMs card
    - Ceramic lead time
  - Initial cost higher

Card Attributes/Life Studies

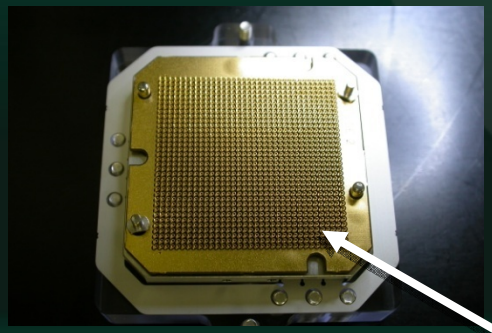
Product Supplied as an Insert Large Version with 780 LGA Points

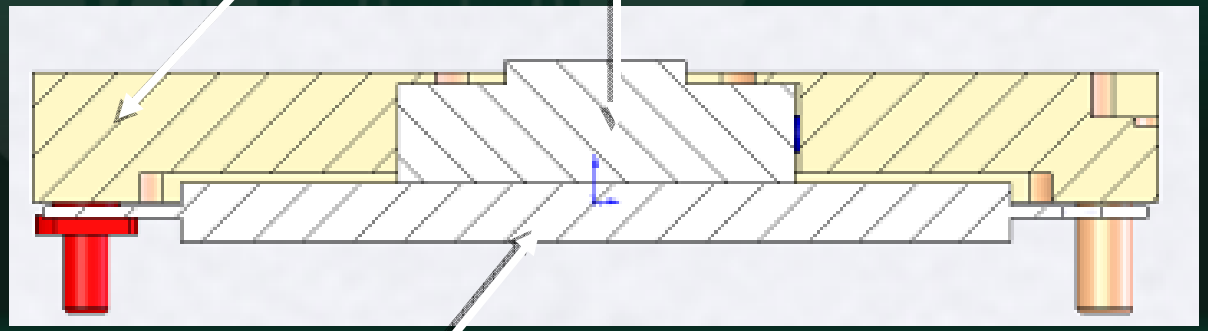


MEMs Springs

Probe Head (PH)

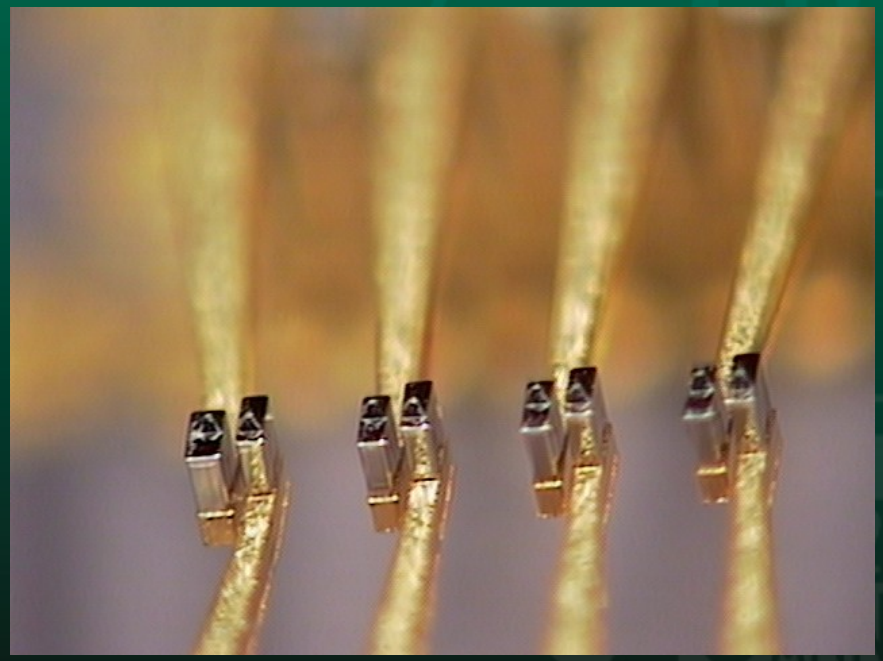
PH Frame





Interposer

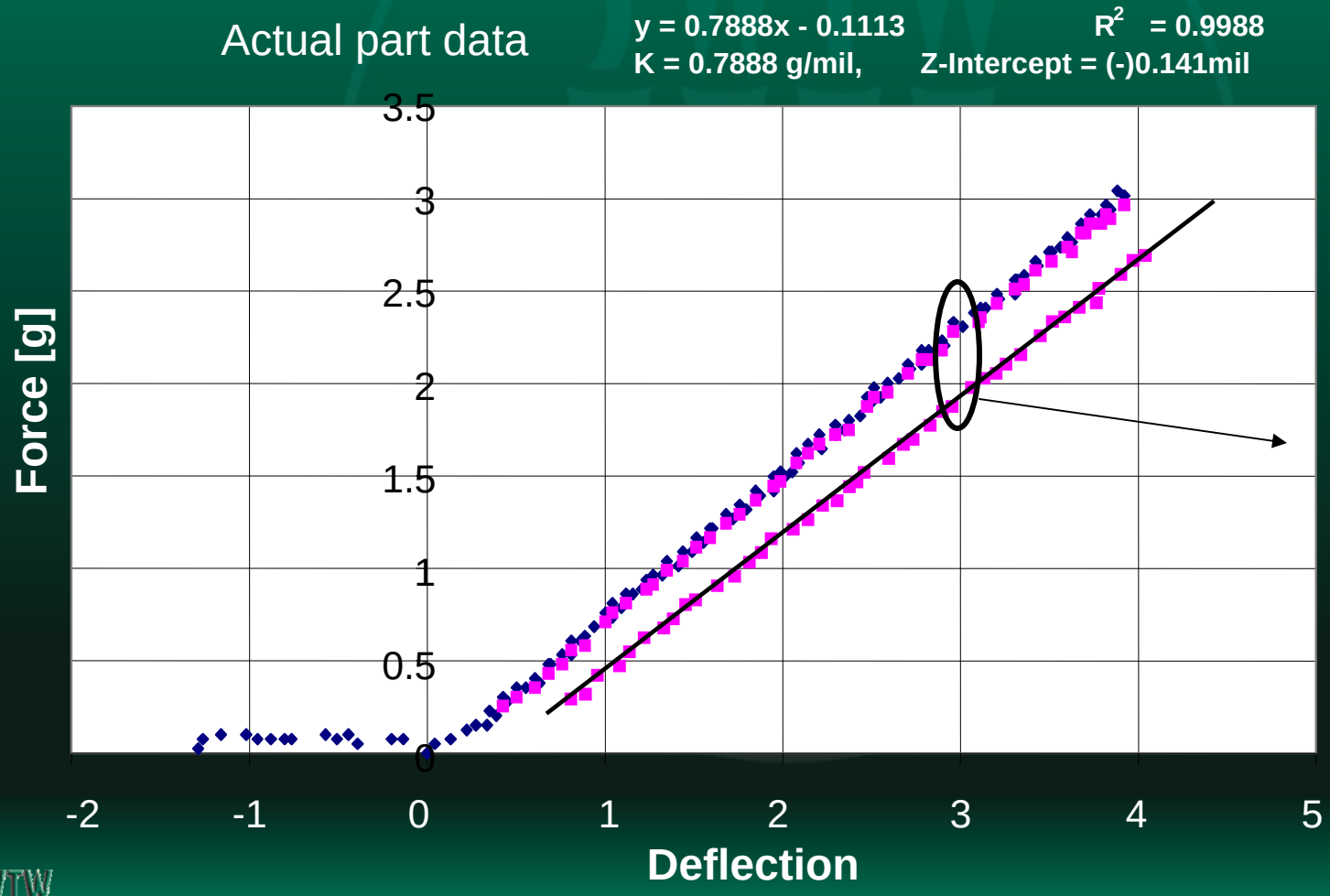
CRES Test Probes Setup Criteria



- **Probe Tip 20um**
- **Probe Force 1.2g/mil**
  - Meets SUP (Structure Under Pad) specification
- **Over travel 1 to 4 mils Max**
- **Tested OT 2 and 3 mils**
  - Optimum CRES at 3 mils
- **Single touchdown**

MEMS Low Probe Force

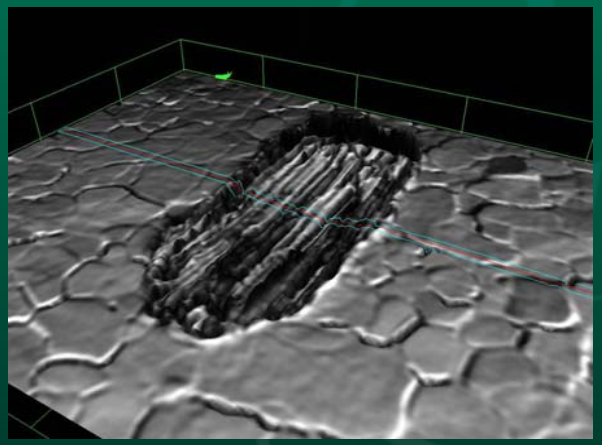
Spring Force vs. Deflection

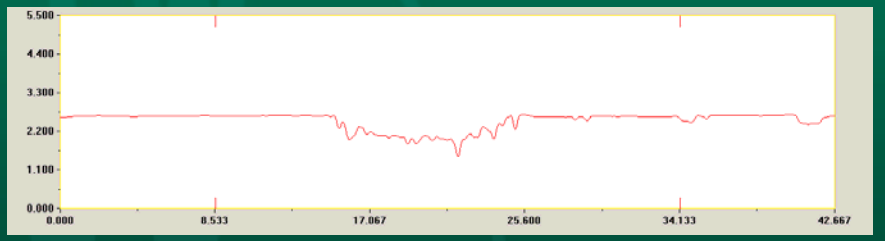


Std. Cantilever probes are 2.5g/mil OD or 7.5grams at program OD

At Max OD force = 2.4 grams

Typical 3D Image, Line Profile (center die) and Measurements (all)

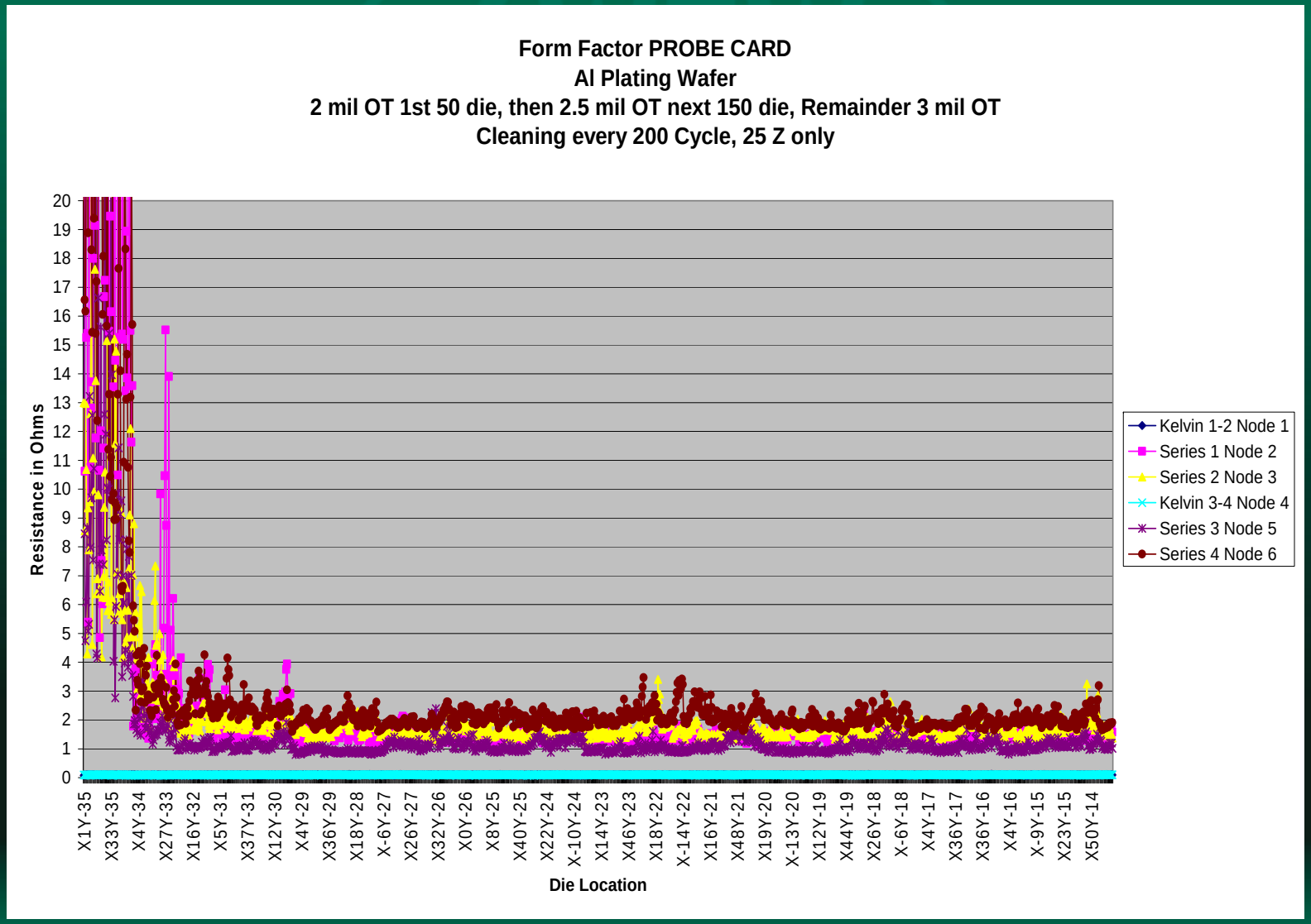




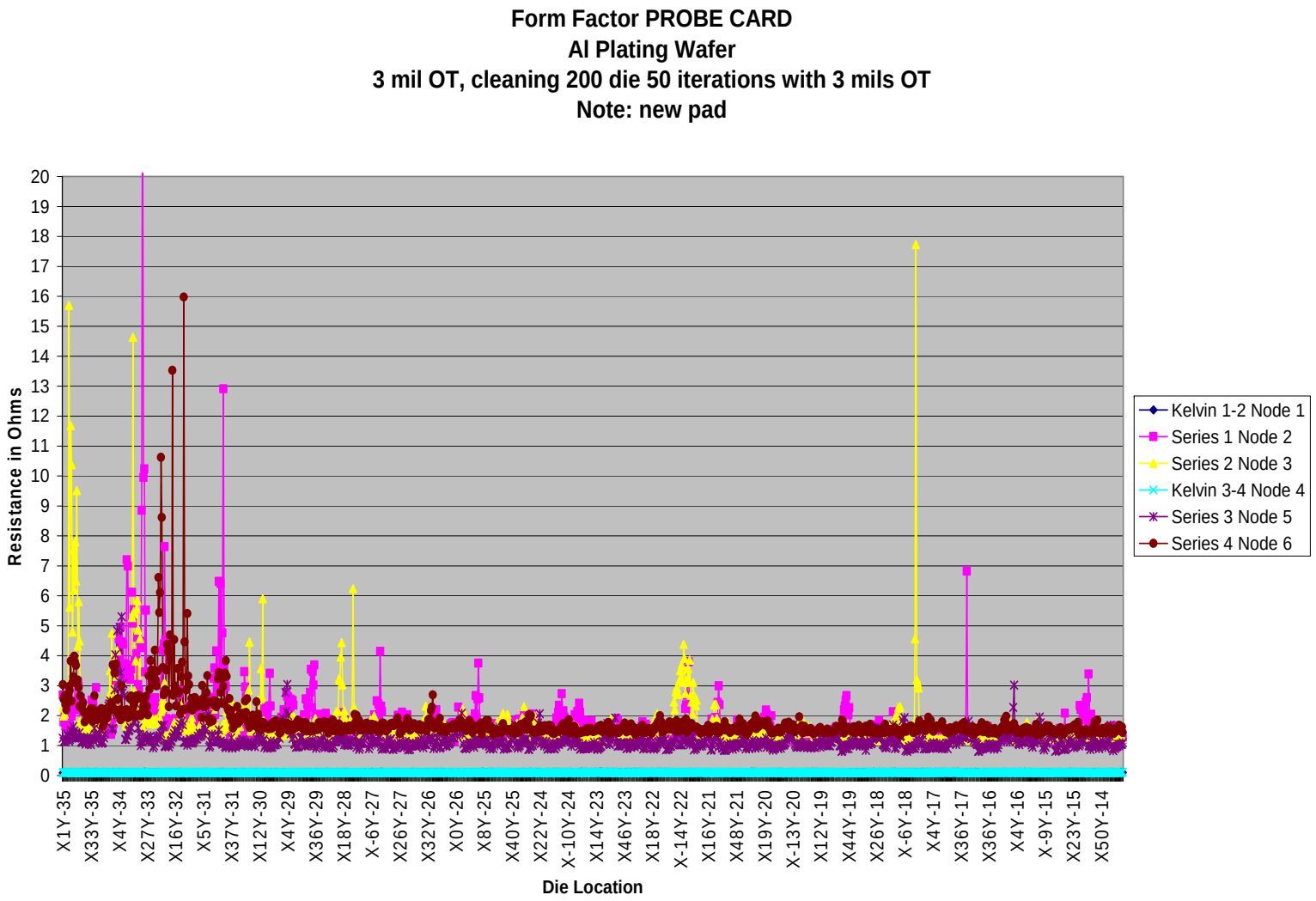
Total Average = 0.78µm (0.0308mils)

	top right	top left	top	right	left	center	bot right	bot left	bot
Average	0.74	0.6927	0.8912	0.8438	0.7687	0.703	0.7082	0.804	0.8683
Max.	1.145	0.778	1.169	0.974	0.932	1.126	0.948	0.963	1.121
Min.	0.562	0.573	0.494	0.68	0.624	0.573	0.493	0.646	0.689
Range	0.583	0.205	0.675	0.294	0.308	0.553	0.455	0.317	0.432
Sigma	0.218	0.0724	0.2224	0.1261	0.1105	0.2112	0.1535	0.1271	0.1713
3 Sigma	0.6541	0.2173	0.6671	0.3782	0.3316	0.6336	0.4605	0.3813	0.514

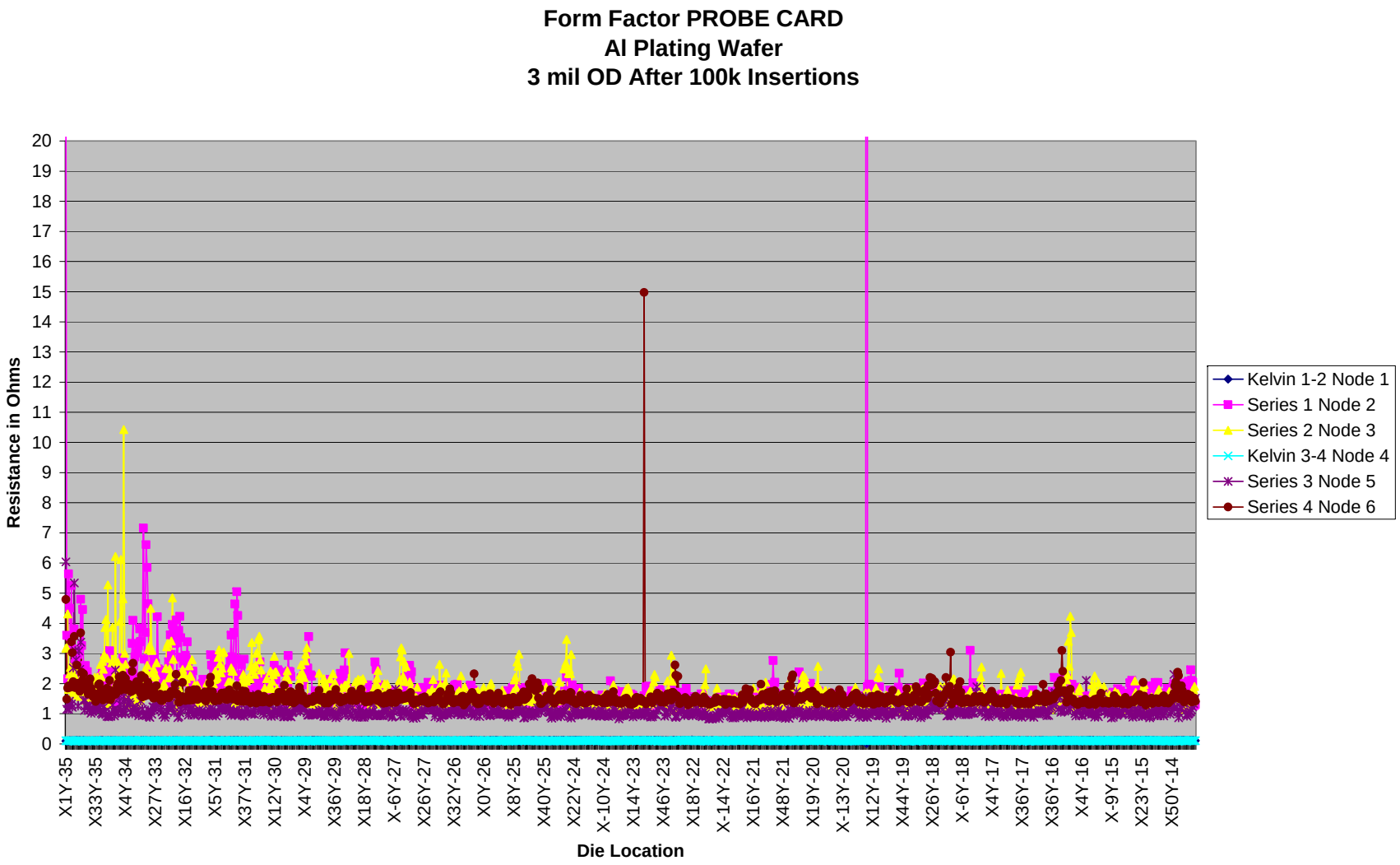
Optimizing CRES, with Cleaning and OT



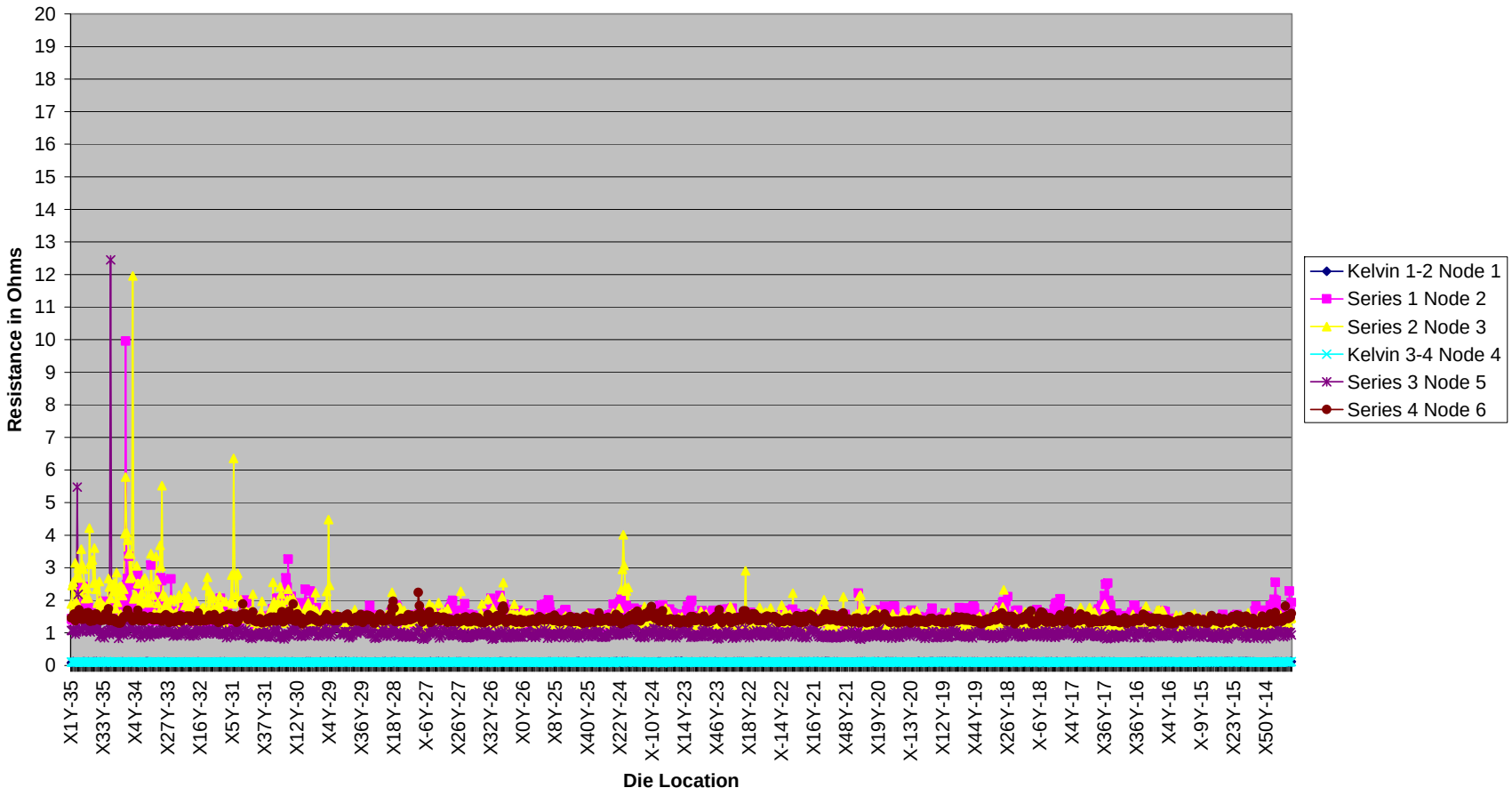
CRES with Optimized Cleaning and OT



MEMS CRES after 100k + Insertions

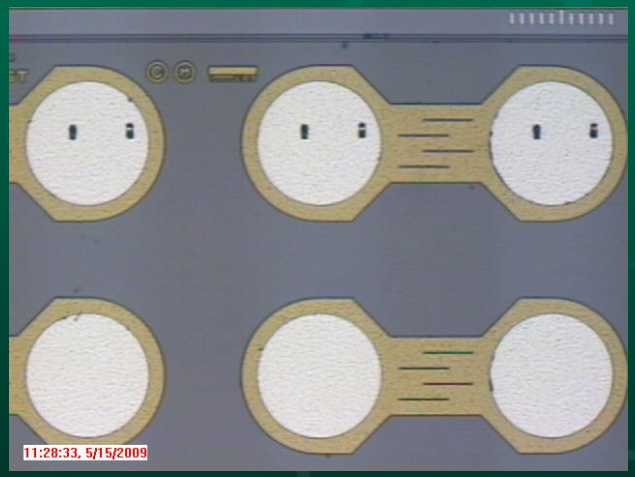


MEMS After 300k Insertions

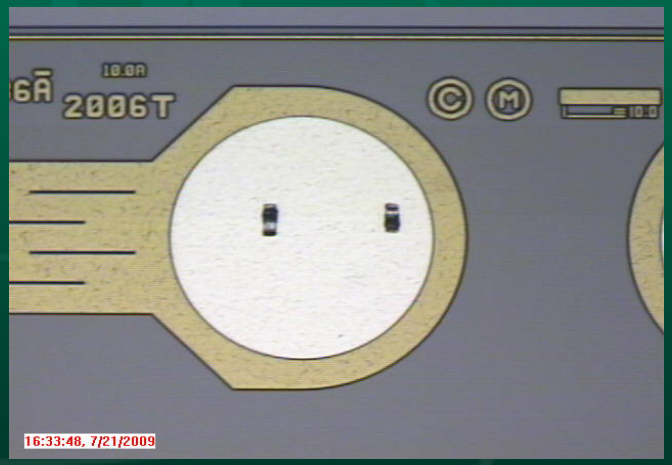


MEMS Probe Marks

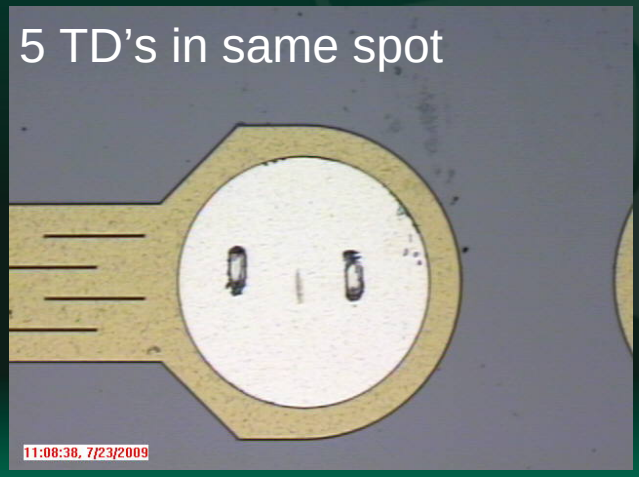
New Card



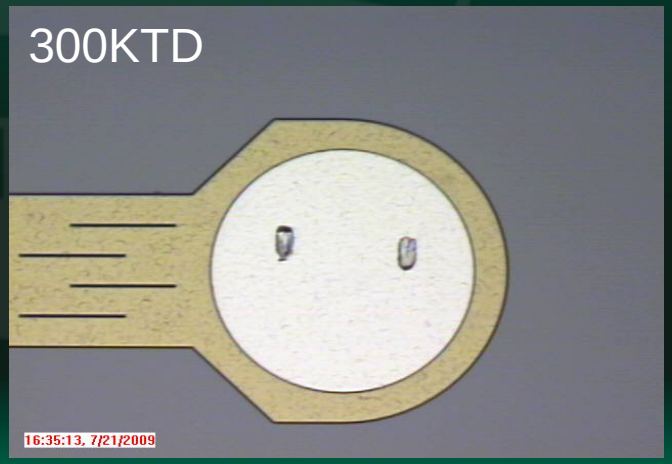
100K TD



5 TD's in same spot

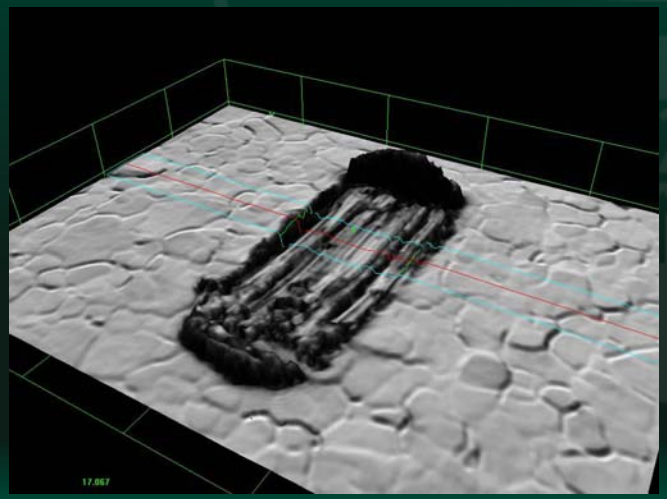


300KTD



MEMS Life Test

- Probe card life test through 375k insertions
- Cres Stable through 375k insertions
- Probe card wear minimal



Cost Of Ownership

Key Ideas for Cost Model

- Drive more test to wafer sort to yield at lower cost point
- Shmoo Volume, Package Cost, and yield variance to cantilever sort to determine value proposition

Key Cost Drivers

- **Sort Yield**
  - Test Everything at Wafer Sort
- **Final Yield**
  - Reduce Cost of Test at Final
- **Package Cost**
  - Reduce Package Scrap
- **Test Costs**
  - Sort typically costs less than FT

Cost Model for Power Management

5% better overall yield at Final Test

10	Total Program Wafers
400	Die per Wafer
400	TD's wafer (3X3mm die, 3000 dpw, 1//)
1000000	Card Life FFI
1000000	Card Life Cantiliever
2	Peak Card Usage

Probe Card Costs				***Test Cell Efficiency***				***Yield Benefit***		
	Cantiliever	FFI			Cantiliever	FFI			Cantiliever	FFI
Initial PCB Cost	3000	3000		Total Program Wafers	10	10		***Wafer Yield***		
NRE	150	3500		Sort Steps	1	1		Wafer Cost	$ 726	$ 726
Spider/PH	1300	5000		Touch Down's/Wafer	400	400		Avg Yield	100%	89%
Cards Needed[1]	2	2		Avg Tech & Eng Labor	25	25		Program Wafers	10	10
Initial Card Cost	2750	13500		Test Cell Cost/sec	0.01	0.01		Yield Advantage		0
# Rebuilds	0	0		Total Program TD's	4,000	4,000		Yielded Die	4,000	3,560
Cost/Rebuild	1300	3000		On-Line Clean Cycle	100	100		Effective Wafer Yielded		-11%
Rebuild Cost	0	0		On-Line Clean Time	10	10		Yield Loss $'s	$ -	$ (79.86)
# Repairs	5	2		Total On-Line Clean $	4	4		***FT Yield***		
Avg. Repair Cost	500	1000		MTTA	25000	25000		FT Yield Loss	25.0%	9%
Repair Cost	2500	2000		Response Time (min)	15	15		Yield Loss	1,000	320
				Test Cell Wait Cost	1.44	1.44		Test Cost/Unit + Die Cost	235.56	235.56
				Off-Line Maint Freq	100000	100000		Pckg cost/Unit	37.20	37.20
				Avg Off-Line Cost	20	20		Cost of Scrap	$272,760	$87,392
				Cost of Off-Line Maint	0.8	0.8		Total Cost of good units	818280	883633.296
Total Cost of Scrap	$5,250	$15,500			$6	$6			$272,760	$87,312
Cost Benefit using FFI		($15,500)				$0				$185,448
Total Benefit/(Cost) of FFI vs. Other										$169,948

Cost Model for ADC

TDs Wafer	3000
Sort Steps	1
Total TD/Wafer	3000
Card Life FFI	1000000
Card Life Other	500000
Peak Card Usage	2

Received a $132K cost benefit by switching to MEMS

Probe Card Costs

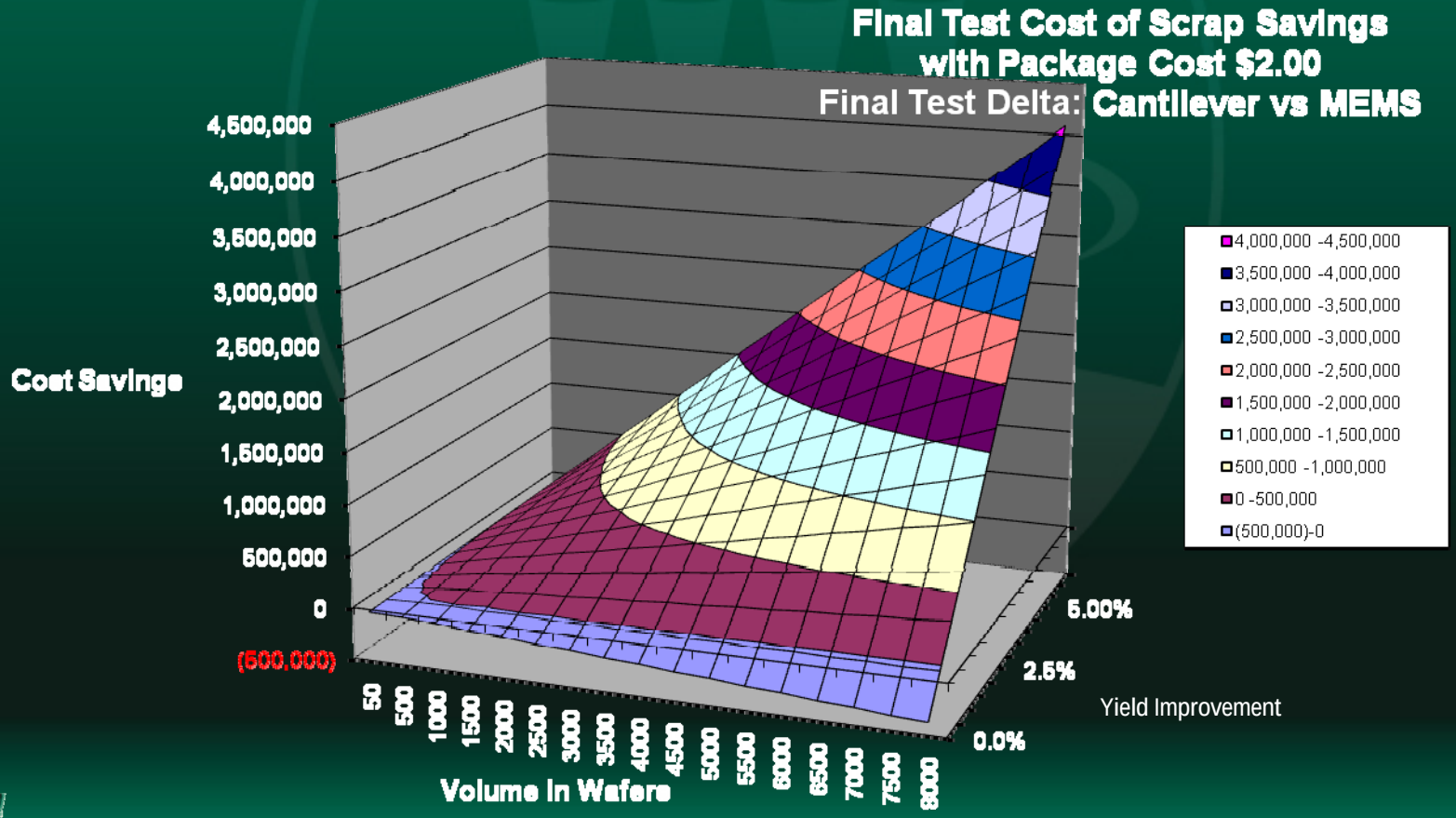
Cantilever	FFI	
$3,000	$3,500	Initial PCB Cost
$150	$3,500	NRE
$1,300	$5,000	Spider/PH
2	2	Cards Needed[1]
$5,750	$17,000	Initial Card Cost
6	2	# Rebuilds
$1,300	$5,000	Cost/Rebuild
$7,800	$10,000	Rebuild Cost
5	2	# Repairs
$500	$1,000	Avg. Repair Cost
$2,500	$2,000	Repair Cost
$16,050	$29,000	Total Probe Card Spend

Yield Benefit

Cantilever	FFI	
		Wafer Yield
1,500	1,500	Wafer Cost
3,000	3,000	Die Per Wafer
98.0%	98.0%	Base Wafer Yield
0.0%	2.0%	Underkill Identified at Sort
98.0%	96.0%	Final Sort Yield
1,200	1,200	Program Wafers
3,528,000	3,456,000	Yielded Die
$36,000	$72,000	Cost of Yield Loss
		FT Yield
2.0%		Underkill Passed on from Sort
96.0%	98.0%	Final Sort Yield
141,120	69,120	Pkg Part Loss
$0.42	$0.42	Final Test Cost
$0.10	$0.10	Package Cost
$2.00	$2.00	Die Cost
$355,622	$174,182	Cost of Scrap
$391,622	$246,182	Cost of Yield Loss
$407,672	$275,182	Yield Loss + Probe Card Spend
	$132,490	(Cost)/Benefit of MeMs

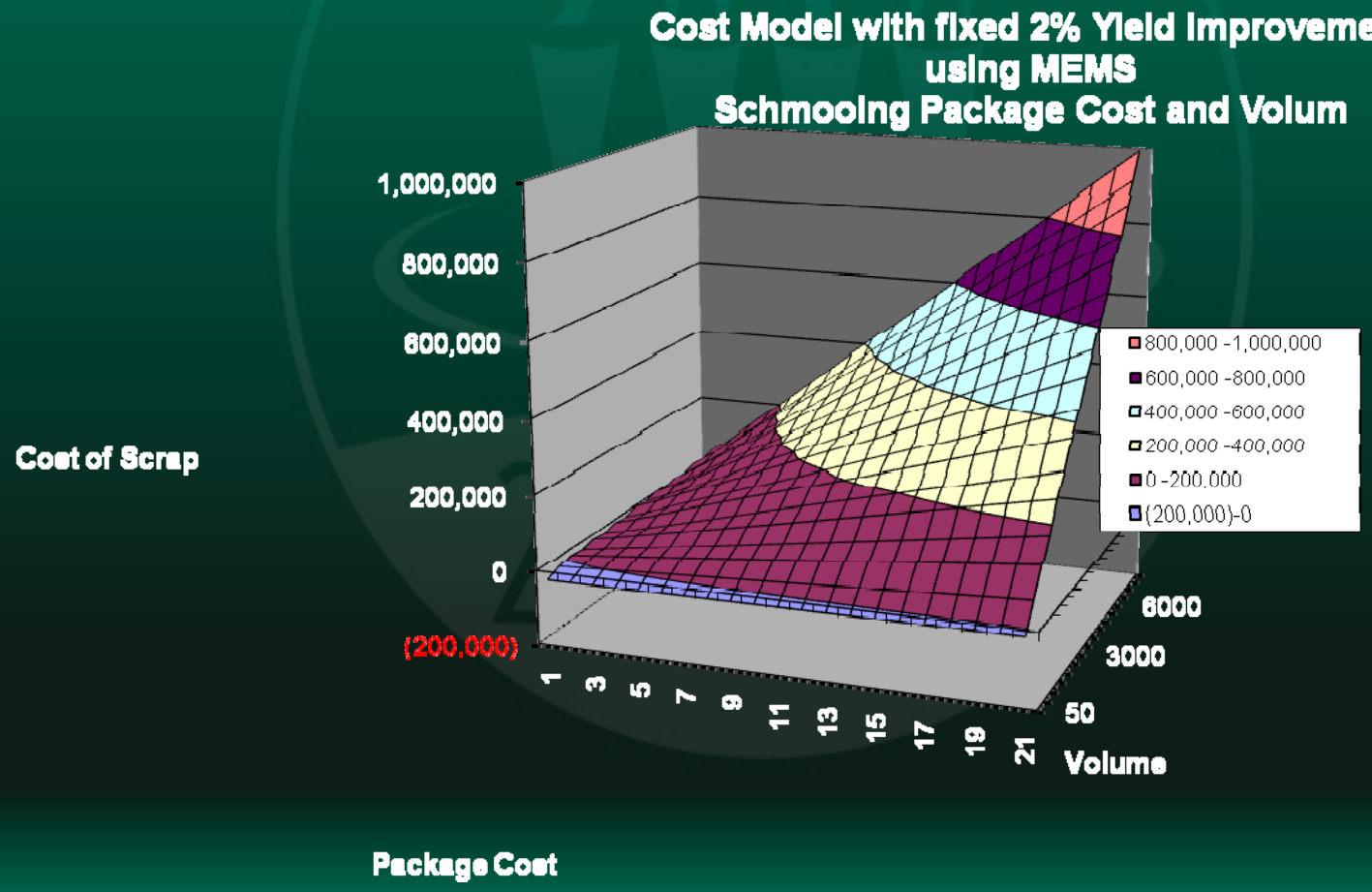
Cost Model for ADC

With > 0.5% yield improvement, MEMs provides cost savings at any wafer volume



Cost Model for ADC

At $0.01 package cost MEMS provides cost benefits at >500 wafers



Next Steps

- **Carry on to 1 million insertions or breaking point**
  - Compare to Cantilever life
- **Vary cleaning process to optimize cycles between cleaning**
  - By process
- **CRES Study with Higher current**
- **Release to High Volume Manufacturing**

Summary

MEMS Probes Support

- **MEMS probes enable full electrical test at Wafer sort**
  - Better FT yields and less scrap
  - Initial product showed 6% FT yield improvement
- **Supports MCM, and SIP programs**
  - Testing Everything at Wafer Sort improves module yields
- **Improve Known Good Die Test capability and sales**
- **EZ Implementation in manufacturing**
- **High Current Capable over 650ma per pin**
- **High Speed capable over 1.6ghz test limited by product**

Acknowledgements

- Dale Anderson
- Jessica Nguyen
- Shalabh Goyal
- Hemang Dave
- John Hsia
- Dane Granicher –FormFactor